

RF to Millimeter-Wave Front-End Component Design Trends for 5G Communications

With Cadence AWR Software

RF front-end architectures grow more complex with each generation of communication systems. To accommodate these architectures, more densification and miniaturization is taking place with electronic systems implemented through innovations in system-in-package (SiP) design. Cadence offers the broadest, most integrated design solution to bring the Intelligent System Design™ strategy to the communication products of the future.

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Overview

With the release of each new generation of wireless technology since the introduction of the portable phone in the early 1980s, mobile communications have progressed exponentially. Each generation has launched new services and business opportunities, leading up to what is being referred to as the “Third Wave” of communications. The evolution, made possible through 5G and future 6G technology, will support even more new services for industry and society well into the 2030s and beyond (Figure 1).

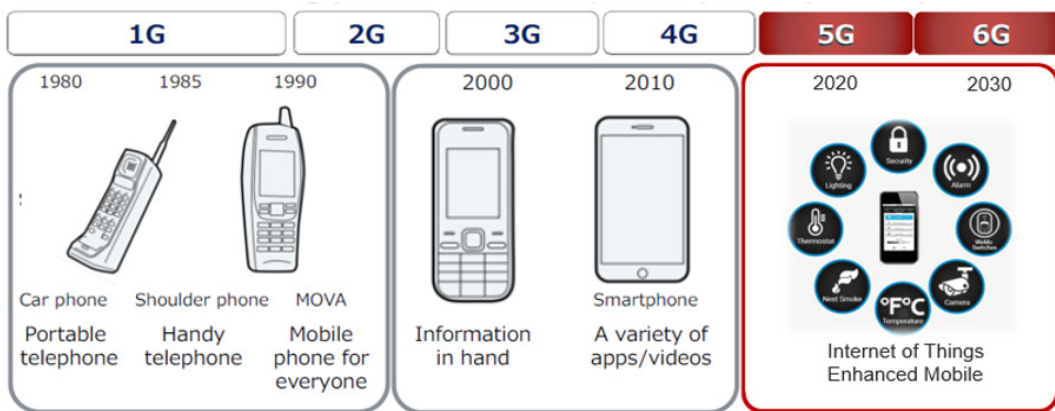


Figure 1: Generations of mobile communications technology and services

5G represents the first step towards this next wave of services with expanded connectivity and a significant upgrade in multimedia capabilities combined with artificial intelligence (AI) and the internet of things (IoT). 5G will be the first generation of mobile communications to utilize millimeter-wave (mmWave) band frequencies, supporting bandwidths of several hundred megahertz (MHz), which will actualize ultra-high-speed wireless data communications of many gigabits per second.

This white paper discusses related design challenges and solutions, presenting several case studies where the Cadence® AWR Design Environment® platform has been used to develop products for this third wave of communications. Examples include a multiband active antenna tuner for cellular IoT machine-type communications (mMTC) applications, a linear power amplifier (PA) design flow to address enhanced mobile broadband communications in the sub-6GHz bands, and a 5G mmWave (28GHz) reference design being developed by Cadence (Figure 2) with multiple design tools for a complete chip, package, board, and antenna design serving 5G fixed wireless access (FWA) application.

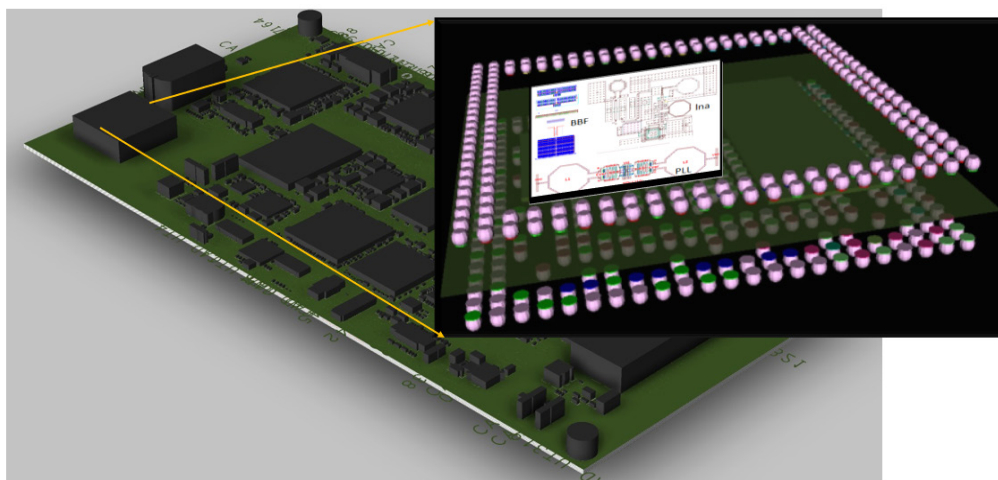


Figure 2: 28GHz 5G reference design including PCB, package (interposer) on package (LTCC), and 45nm RFIC

The Third Wave of Wireless Communications

5G and subsequent systems will close the gap between the physical and cyber worlds. Today, mobile consumers use wireless connectivity to access the web from almost any location. In the future, high-speed coverage will be more widespread and faster, and there will be greater emphasis on uplinking information from real-world events and human and/or internet of things (IoT) activity to the internet.

Once this information is in the cloud, AI can reproduce the real world in cyberspace and emulate it beyond physical, economical, and time constraints, so that “future prediction” and “new knowledge” can be discovered and shared. The role of wireless communications in this cyber-physical fusion is assumed to include high-capacity and low-latency transmission of real-world images and sensing information, and feedback to the real world through high-reliability and low-latency control signaling.

Radio communications in this cyber-physical fusion scenario corresponds to the role of the nervous system transmitting information between the brain and the body. Communications convert real-world events to the cyber world through enhanced uplink capabilities and feedback information provided to humans and devices through low-latency downlink functionality.

The next wave of communications focuses on the three areas of service shown in Figure 3:

- ▶ Enhanced mobile broadband (EMBB) extends the current mobile experience with high data throughput on the order of more than 10Gbps, high system capacity on the order of more than 1000 times that of LTE, and a much better spectral efficiency than LTE (3-4 times that of LTE). Its use cases are high-speed mobile broadband and virtual reality, augmented reality, gaming, etc.
- ▶ Ultra reliable low latency services (URLLS) focuses on low latency, high reliability, and high availability aspects. The expectation is of the order of less than one millisecond of latency and availability on the order of 99.9999%. This is basically for mission-critical use cases and applications.
- ▶ mMTC provides connectivity to a huge number of devices whose traffic profile is typically a small amount of data spread sporadically. So latency and throughput are not a big concern: The main concern is the optimal power utilization of those devices because they are battery powered and the expectation of battery life is around 10 years or so.

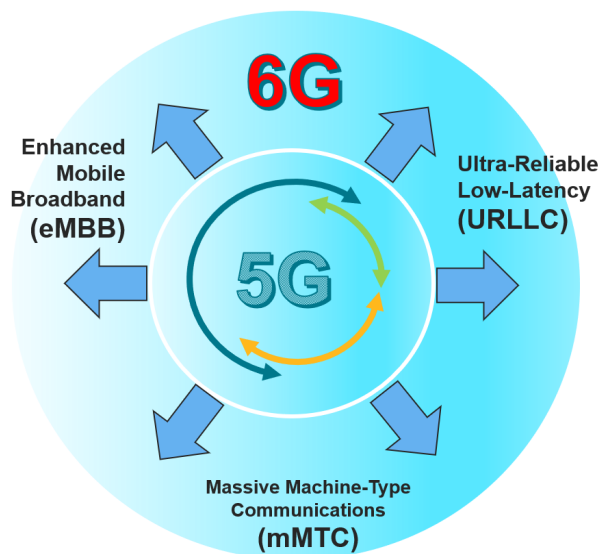


Figure 3: New business services enabled with the third wave of communications, initiated with 5G

Current 5G activity in mmWave front-end design includes development of beam steering phased arrays, antenna-in-package (AiP) solutions, beamforming RF integrated circuits (RFICs), multi-technology integration, and new linear power amplifier (PA) architectures. Early 5G deployment and related trials have shown room for improvements in coverage and uplink performance in non-line-of-sight (NLOS) environments and heavy traffic use cases. While future system-performance goals are still in the early phases of consideration, there remains a need for continued enhancements in order to fully achieve the promise of this next wave of communications. Extreme performance is needed to provide the high reliability and low latency that will close the gap between the cyber and physical worlds.

6G will implement many different technologies to close this gap, including new topologies of overlapping cells with distributed networks of beamforming antennas controlled by artificial intelligence (AI) and machine learning (ML) to select optimum transmission paths dynamically. Previous cellular communications were based on networks of hexagonal cells spaced far enough apart to avoid signal interference with neighboring cells. 6G may employ a spatially non-orthogonal, overlapped, and dynamic topology to increase path selection. Beam control through AI/ML will help reduce intercell interference (ICI) at a cost of complexity. This architecture will also require new antenna designs, conformal as well as phased arrays.

For more bandwidth, 6G is expected to utilize higher mmWave frequencies from 94GHz to 3THz. The move to higher frequency bands will help reduce the size of these antennas, making efforts to shrink component footprints easier; however, the antennas, feed networks, and package interconnects will be more susceptible to parasitics and unintended coupling (crosstalk), requiring rigorous EM analysis and design verification at a system level, as shown in Figure 4.

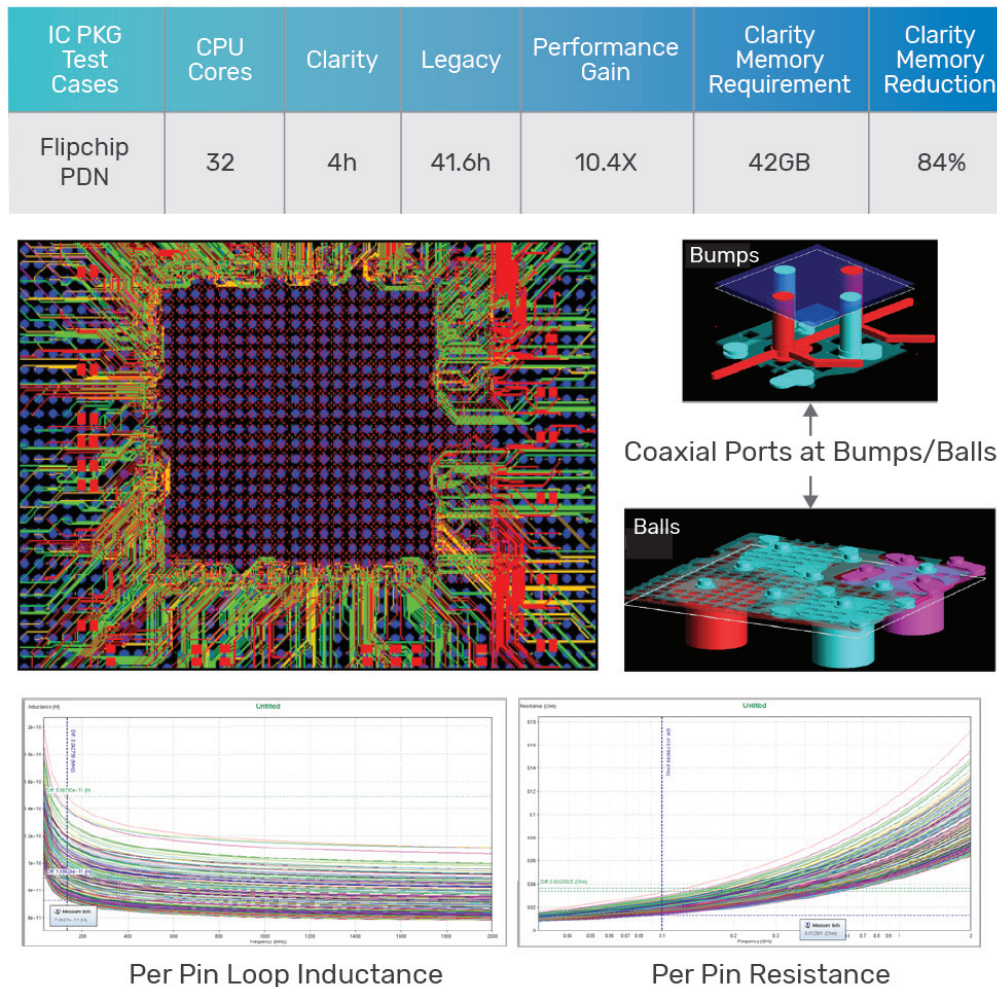


Figure 4: The Clarity 3D Solver (finite element method [FEM]/finite difference time domain [FDTD]) addresses critical interconnect modeling of large-scale, integrated RF/mixed-signal electronic systems powering third-wave communications

New functionality in spatial multiplexing and massive multiple in-multiple out (MIMO) are under investigation including the use of reflective surfaces and metamaterials to manage signal propagation in crowded urban environments with limited line of sight. Coverage will be expanded through space, sea, and high-altitude drones.

Lastly, much of the focus will be on physical design of radio access front ends. Strategic design partitioning, leveraging of optimal semiconductor processes, and multi-fabric assemblies will undoubtedly be utilized, calling for a range of simulation technologies, design and manufacturing flows, and tool interoperability. All these trends were anticipated in the development of Cadence's Intelligent System Design strategy to support co-design and co-optimization of next-generation wireless electronic systems across multiple domains, including RF, analog, and digital simulation, aided by large-scale electromagnetic (EM) and thermal analysis, and robust design verification and signoff.

Addressing RF Front-End Physical Design

The push toward mmWave, driven by the need for more available bandwidth, introduces higher propagation losses and smaller geometries. To address greater propagation losses at higher frequencies, 5G and subsequent networks will employ more efficient, intelligent antennas based on MIMO and beam steering phased array technologies. Phased array technology, adopted from expensive aerospace applications, will need to transform into small form factors and cost-effective solutions for commercial use.

Meanwhile, advanced modulation and coding schemes will provide greater spectral efficiency at the cost of higher peak-to-average power ratios (PAPR), putting pressure on PA designers that must simultaneously achieve high linearity and drain efficiency. Hybrid digital/RF front-end architectures will continue along a development path that supports beam steering, multiple transmit/receive (TX/RX) channels and frequency bands, advanced modulation schemes, and amplifier linearization techniques. At the core of these networks will be highly integrated RFICs/monolithic microwave ICs (MMICs), modules, and RF/mixed-signal PCB systems.

With each generation of a communication system, RF front-end architectures grow more complex to support all these requirements. To accommodate these architectures, more densification and miniaturization is taking place with electronic systems implemented through innovations in SiP design (Figure 5). Not only does SiP integrate almost any kind of passive component with the optimum active device, it also supports flexible combinations of analog circuits and RF functions with digital ICs. SiP is a key enabler for portable devices, particularly with respect to the growing number of RF functions that need to be integrated.

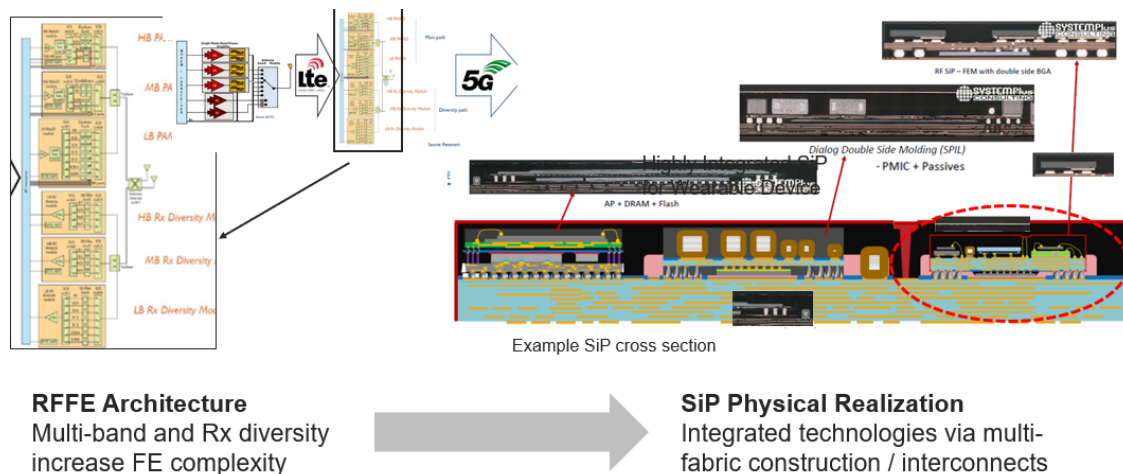


Figure 5: SiP module technology supports complex RF front-end architectures for 5G

A common RFIC and SiP design challenge is concerned with how RF IP blocks are subject to EM, capacitive, supply, and substrate coupling. These potentially harmful interactions result from effects that occur with high-frequency signaling, including:

- ▶ Noise, either into or out of a block, which can travel through the substrate or through power bussing. Placement (floor planning) of noise-generating and noise sensitive blocks is design critical.
- ▶ Parasitic coupling capacitance within/between RF blocks and signals routed nearby (100-1000s of microns away), which can cause disrupted performance.
- ▶ Self-inductance of any nets connected to the RF block.
- ▶ Mutual inductance between any net within an RF block, to nets in neighboring blocks.

RF IP blocks interact much differently than digital IP blocks. Most place-and-route tools are not capable of addressing the unique issues confronted in integrating RF IP. An RF engineer working with RF-aware design tools is required to successfully integrate blocks at the chip, package, or board level. In order to understand the effects of parasitic coupling, either capacitive, inductive, or through the substrate, closed-form distributed transmission-line models and EM analysis are essential for RF IP development. While RF IP blocks will never be as easy to integrate as digital IP blocks, RF design tools will mitigate many of these integration issues.

Cadence RF-to-mmWave Design Solutions

The technical challenges presented by 5G and future 6G development is an extension of what AWR software customers focus on today in the pursuit of higher broadband capacity for greater range resolution in radar applications and high-speed data rates for communications. Throughout the digital communication revolution, Cadence and AWR have been providing electronic design automation (EDA) solutions to support the wireless industry.

Both companies came into existence to address design challenges ushered in by the introduction and mass adoption of EDA. For RF and microwave product development, the AWR® design tools introduced advanced programming technology and a powerful yet intuitive user interface to RF EDA. With the acquisition of AWR, Cadence has added leading RF/microwave design capabilities and expertise to its overall solution.

Cadence solutions cover silicon and compound semiconductor design and simulation software for RF/mixed signal ICs, PCBs, and SiPs. Cadence users also address their EM modeling needs with tools that are fully integrated into Cadence design and manufacturing flows.

For RFIC and module design, the Cadence Virtuoso® RF Solution is built on the Virtuoso System Design Platform and incorporates new co-design capabilities for simultaneous editing of the IC and SiP module, EM analysis solvers to give designers different methods of physical extraction that can easily be entered back into the schematic without breaking the golden schematic, and trusted simulation and analysis engines through our tightly integrated Virtuoso ADE Product Suite and Cadence Spectre® RF Option.

The integration of multiple EM solvers into the Virtuoso RF Solution design environment automates hours of manual work required to run critical passive components and interconnects, enabling engineers to run multiple design experiments in a fraction of the time. The different EM solvers are optimized to address specific design challenges, from full system analysis and design verification to on- and off-chip modeling and passive component characterization.

To address off-silicon RF design, including III-V MMIC and discrete components, modules, and RF board design, the AWR Design Environment platform provides RF system, circuit, and EM design entry and analysis (Figure 6). Cadence AWR Visual System Simulator™ (VSS) communications and radar systems design software is primarily concerned with the top-level radio and radar design, operating from behavioral block models to provide link budget and spurious heritage analysis, as well as time-domain baseband through RF communications/radar system simulation.

AWR VSS software works seamlessly with AWR Microwave Office® software, which supports RF design at the transistor, transmission line, and RF-aware passive component level with frequency domain, nonlinear harmonic balance simulation. AWR Microwave Office software is used for RF front-end component design, including power and low-noise amplifiers, filters, mixers, matching networks, and more. The AWR AXIEM® 3D planar and Analyst™ 3D FEM solvers provide fully integrated EM analysis for antenna design and broadband characterization (S-parameter extraction, far fields, and currents) of passive structures.

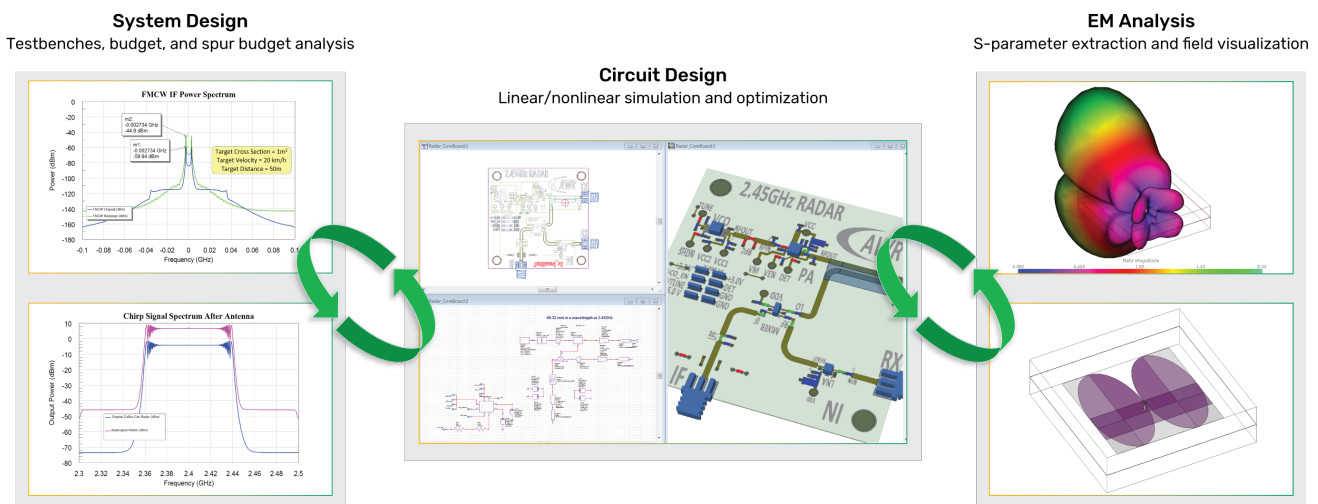


Figure 6. Design solutions in the AWR Design Environment platform

Multi-Band Active Antenna Tuner for Cellular IoT Applications

One goal of 5G mMTC is to provide scalable connectivity for a large number of IoT devices (Figure 7). The devices themselves support various sensing and actuation functionality. They are relatively low in complexity but battery-constrained in order to support years of field operations without servicing. To share data to the network, mMTC is uplink-centric with relatively low data rates, optimized for small packets (down to a few bytes). Uplink communication is based on sporadic user (event-driven) activity or scheduled transmissions.

Today's cellular IoT (cIoT) devices are supported through narrowband IoT (NB-IoT) and LTE Category M-1 (Cat M-1) networks, which currently offer 40,000-50,000 devices per cell. 5G aims to support up to 1M devices per cell. Being tied to a cellular network gives them greater range than low-power wide area networks (WAN), so they are applicable to mobile applications, such as in-transit asset tracking. As sensing devices without the need for time-sensitive information, mMTC networks can be latency agnostic.

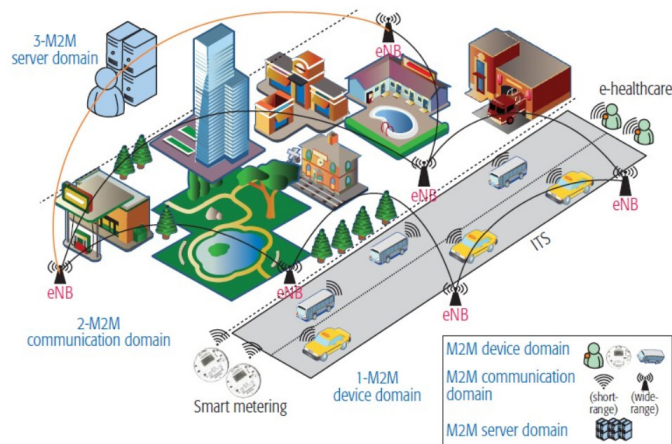


Figure 7: mMTC provides scalable connectivity for a large number of IoT devices (image courtesy of ABI Research)

Fractus Antennas, a leader in the design and manufacture of miniature antennas for smartphones, short-range wireless, and connected IoT devices, uses AWR software to integrate antennas into these products. With the Network Synthesis wizard option available in the AWR Microwave Office software, Fractus Antenna engineers can easily implement a suitable matching network for the desired single-, multi-, or broadband operations. This ensures maximum power delivered to the antenna for devices that require low power consumption without sacrificing range (coverage).

Fractus Antennas designed a multi-band active antenna tuner for a battery-operated prototyping platform for cellular IoT (cIoT) from Nordic Semiconductor. The Nordic Thingy:91 prototyping board in Figure 8 is built around a low-power SiP module (nRF9160) with integrated LTE-M/NB-IoT modem and GPS. Certified for a broad range of LTE bands globally, the Nordic Thingy:91 can be used just about anywhere in the world. The cellular communication can be interleaved with GPS positioning acquisition for sophisticated asset-tracking.

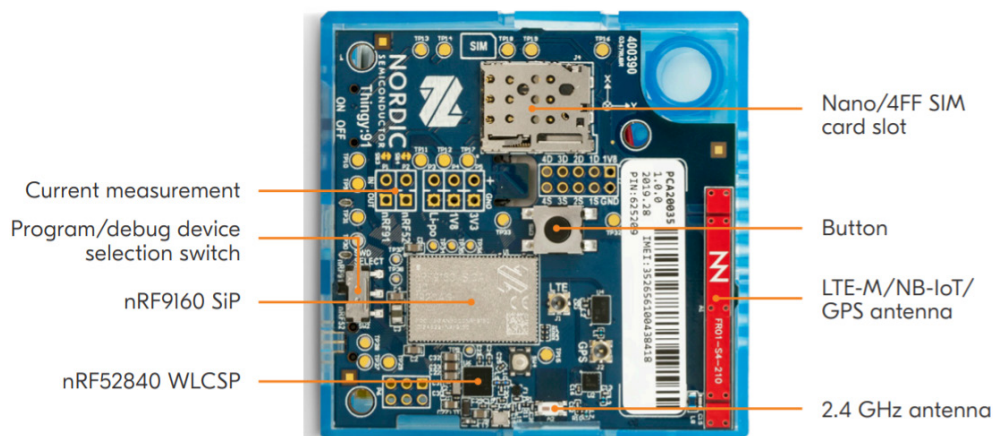


Figure 8: Nordic Thingy:91 prototyping board for cIoT asset-tracking applications (image courtesy of Nordic Semiconductor)

The cloT module and prototyping board offer six bands of operation, including GPS, supported by the antenna and the band-specific impedance matching networks developed by Fractus Antenna. The RF section of the board includes the IoT module from Nordic Semiconductor and two single pole, 8-throw switches from Qorvo, which allow the signal to pass through different matching circuits dependent on the desired operating band and the Fractus Antenna (Figure 9).

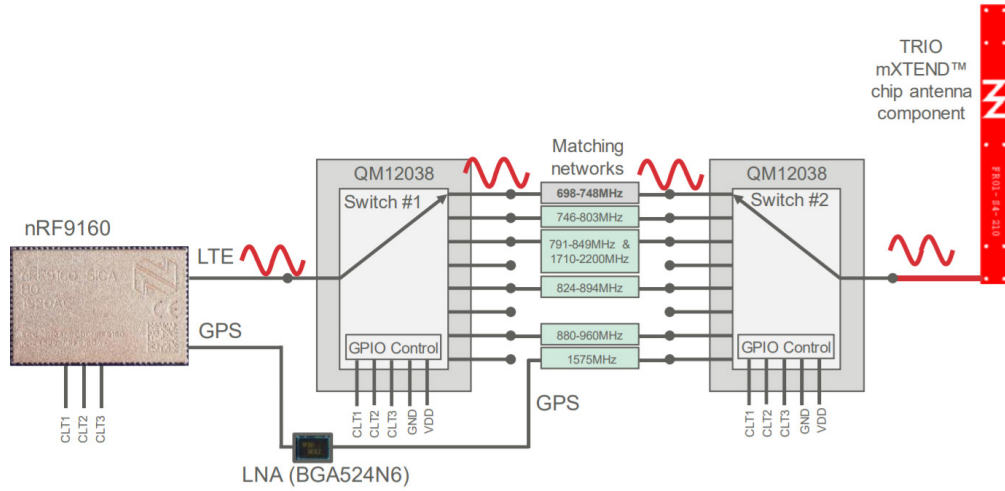


Figure 9: Block diagram of cloT module and active antenna tuner for six-band operations (image courtesy of Fractus Antenna)

The derived matching circuit topologies and bill of materials (BOM) are shown in Table 1 and the resulting antenna efficiency response versus frequency for different switch settings is shown in Figure 10.

STATE	Frequency band	Matching Network									
RF5	698-748MHz & 1710-2200MHz	<table border="1"> <tr><th>Component</th><th>Value</th><th>Part Number</th></tr> <tr><td>Z₁</td><td>5.1nH</td><td>LQW03AW5N1J00</td></tr> <tr><td>Z₂ (C10)</td><td>5.5pF</td><td>GJM0332C1H5R5WB01</td></tr> </table>	Component	Value	Part Number	Z ₁	5.1nH	LQW03AW5N1J00	Z ₂ (C10)	5.5pF	GJM0332C1H5R5WB01
Component	Value	Part Number									
Z ₁	5.1nH	LQW03AW5N1J00									
Z ₂ (C10)	5.5pF	GJM0332C1H5R5WB01									
RF7	746-803MHz & 1710-2200MHz	<table border="1"> <tr><th>Component</th><th>Value</th><th>Part Number</th></tr> <tr><td>Z₁</td><td>4.7nH</td><td>LQW03AW4N7J00</td></tr> <tr><td>Z₂</td><td>0Ω</td><td>-</td></tr> </table>	Component	Value	Part Number	Z ₁	4.7nH	LQW03AW4N7J00	Z ₂	0Ω	-
Component	Value	Part Number									
Z ₁	4.7nH	LQW03AW4N7J00									
Z ₂	0Ω	-									
RF8	791-849MHz & 1710-2200MHz	<table border="1"> <tr><th>Component</th><th>Value</th><th>Part Number</th></tr> <tr><td>Z₁</td><td>9.2pF</td><td>GJM0332C1E9R2WB01</td></tr> <tr><td>Z₂</td><td>6.2nH</td><td>LQW03AW6N2J00</td></tr> </table>	Component	Value	Part Number	Z ₁	9.2pF	GJM0332C1E9R2WB01	Z ₂	6.2nH	LQW03AW6N2J00
Component	Value	Part Number									
Z ₁	9.2pF	GJM0332C1E9R2WB01									
Z ₂	6.2nH	LQW03AW6N2J00									
RF3	824-894MHz	<table border="1"> <tr><th>Component</th><th>Value</th><th>Part Number</th></tr> <tr><td>Z₁</td><td>1.5pF</td><td>GJM0334C1E1R5WB01</td></tr> </table>	Component	Value	Part Number	Z ₁	1.5pF	GJM0334C1E1R5WB01			
Component	Value	Part Number									
Z ₁	1.5pF	GJM0334C1E1R5WB01									
RF1	880-960MHz	<table border="1"> <tr><th>Component</th><th>Value</th><th>Part Number</th></tr> <tr><td>Z₁</td><td>2.5pF</td><td>GJM0335C1E2R5WB01</td></tr> <tr><td>Z₂</td><td>Open circuit</td><td>-</td></tr> </table>	Component	Value	Part Number	Z ₁	2.5pF	GJM0335C1E2R5WB01	Z ₂	Open circuit	-
Component	Value	Part Number									
Z ₁	2.5pF	GJM0335C1E2R5WB01									
Z ₂	Open circuit	-									
RF4	GPS (1575MHz)	<table border="1"> <tr><th>Component</th><th>Value</th><th>Part Number</th></tr> <tr><td>Z₁</td><td>2.2nH</td><td>LQW15AN2NC10</td></tr> <tr><td>Z₂</td><td>2.5pF</td><td>GJM1555C1H2R5WB01</td></tr> </table>	Component	Value	Part Number	Z ₁	2.2nH	LQW15AN2NC10	Z ₂	2.5pF	GJM1555C1H2R5WB01
Component	Value	Part Number									
Z ₁	2.2nH	LQW15AN2NC10									
Z ₂	2.5pF	GJM1555C1H2R5WB01									
RF2&6	available for other bands	empty									

Table 1: Fractus Antenna matching circuit topologies and BOM (image courtesy of Fractus Antenna)

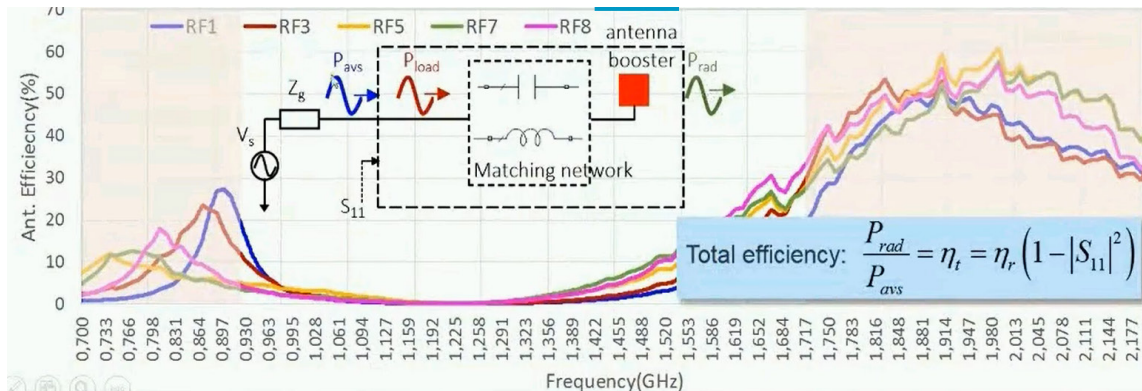


Figure 10: Antenna efficiency response vs. frequency for different switch settings

The impedance matching networks are developed with the AWR Network Synthesis wizard. This goal-driven synthesis tool creates matching networks according to simulation measurements and user specified performance goals such as small-signal return loss or nonlinear amplifier behavior (Pout, PAE, etc.) from load-pull performance contours. The synthesis engine uses a proprietary, genetic optimization algorithm and heuristics to identify candidate matching networks, addressing challenging impedance matching problems across multiple performance goals and frequency bands.

The RF designer specifies which component types such as an inductor, capacitor and transmission line can appear in a given series or shunt configuration thereby managing the topology as well as allowing the user to constrain component parameter values to reflect manufacturing tolerances. This capability accelerates impedance matching, providing RF engineers with a greater number of viable network candidates through rapid design space exploration, (Figure 10).

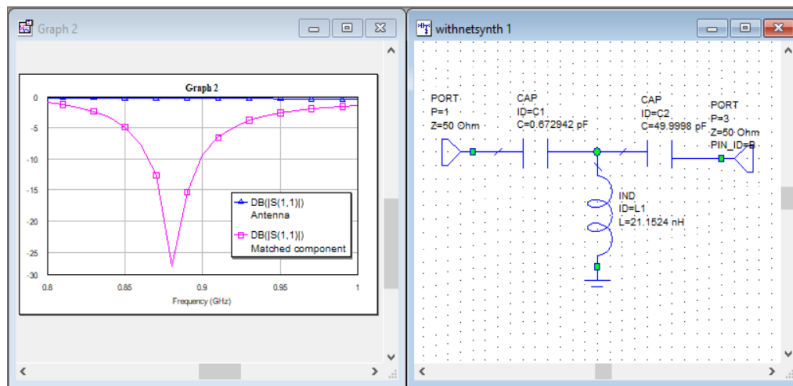


Figure 11: Simple two-element (ideal inductors) matching circuit and resulting return loss of matched antenna component

Synthesized networks can be based on models from the AWR Microwave Office software's ideal parts library, vendor component libraries, and microstrip transmission lines using substrate definitions in the given project. The user can then specify which candidate networks to import directly into the AWR Microwave Office project. Engineers at Fractus Antenna use network synthesis to achieve the desired in-band return loss for their surface mount antenna model which is available as a component model (S-parameters) in the AWR Microwave Office software's standard vendor library. The designer places this antenna component into a schematic subcircuit and develops an impedance matching network to optimize the subcircuit's return loss, thereby maximizing antenna efficiency, the ratio of power radiated to power supplied to the antenna.

In addition to developing the matching network, AWR software and AWR AXIEM analysis can be used to further characterize the board to ensure the matching circuit works properly when incorporated into a larger structure with likely parasitics. To do this, the PCB import wizard in the AWR Design Environment platform was used to import the metal layers, which are available as Gerber layout files from the manufacturer's website. The four individual metal layers were used to create an AWR AXIEM analysis subcircuit combined into a four-layer structure, shown in Figure 12.

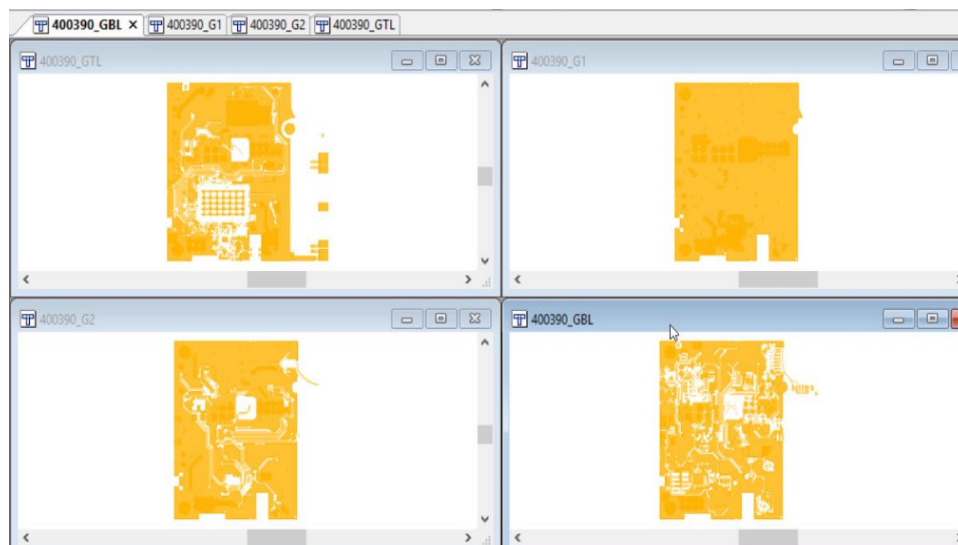


Figure 12: Four-layer (2 signal, 2 ground planes) Gerber file layouts imported into the AWR Design Environment platform

Figure 13 shows the structure in the AWR AXIEM analysis with defined edge ports and annotation of the automatic adaptive meshing used to solve and extract the S-parameters. Shape preprocessing rules were applied to simplify the via structures for faster simulation without sacrificing accuracy. This EM structure size was approximately 84k unknowns and was easily solved in about 10 minutes on a single machine. Looking closely at the mesh, one can see the hybrid meshing technology employed by AWR AXIEM analysis to ensure fast and accurate results.

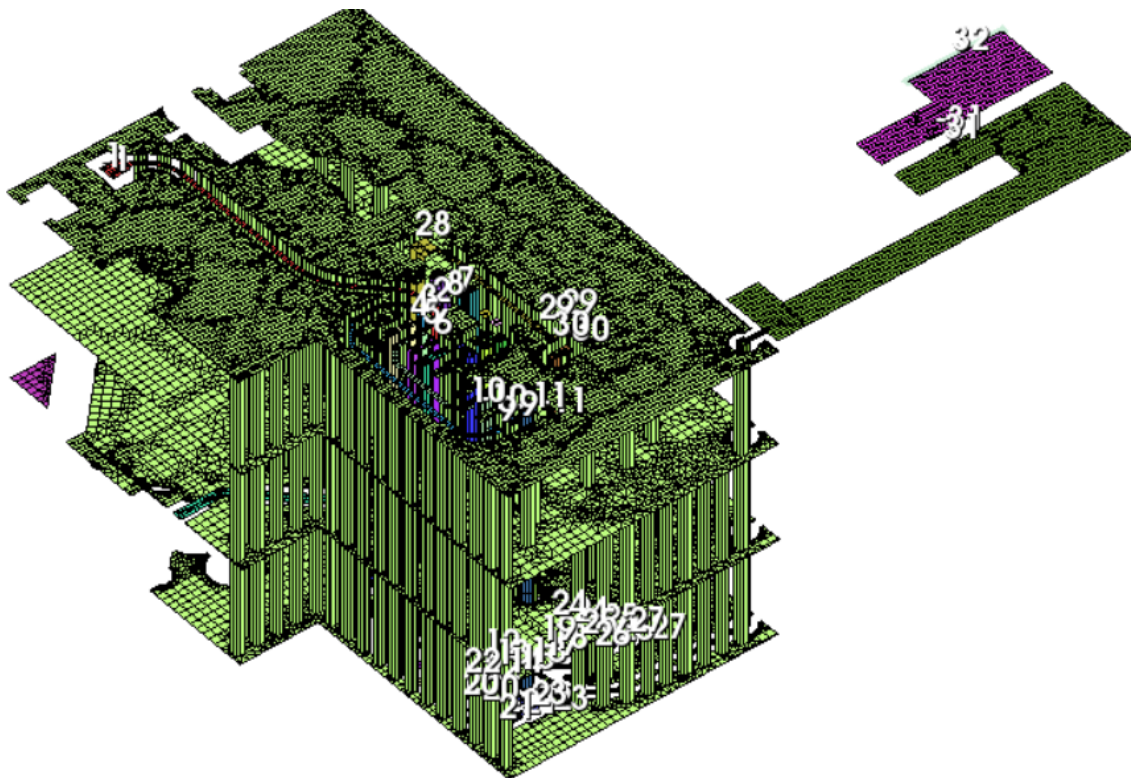


Figure 13: Exploded view of Thingy:91 structure (RF section) in AWR AXIEM software with defined edge ports and annotation showing the automatic adaptive meshing

With the AWR AXIEM analysis fully integrated within the AWR Microwave Office software’s circuit simulator, EM/circuit co-design is achieved by simply placing the subcircuit containing the EM structure into an AWR Microwave Office schematic with other circuit-based components (Figure 14).

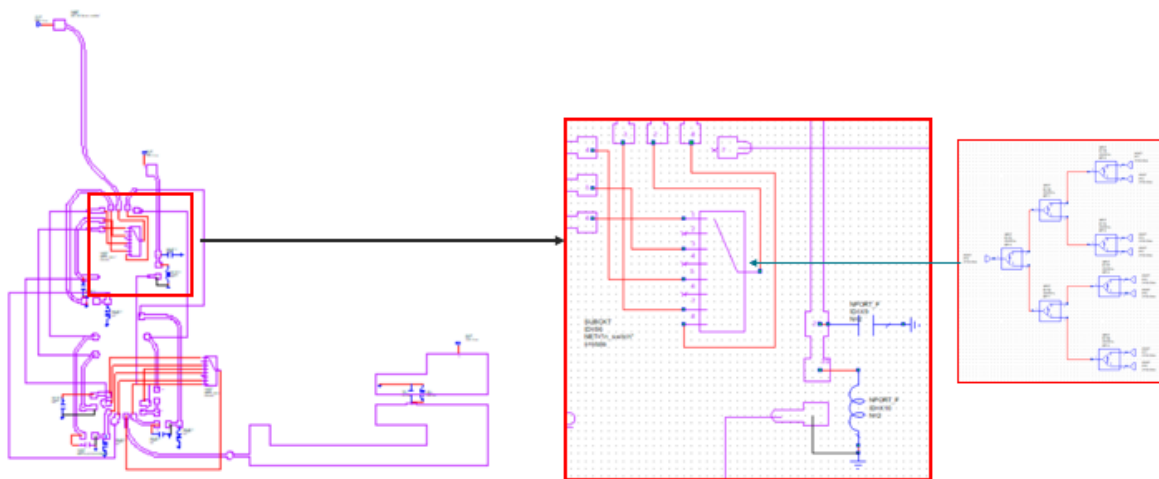


Figure 14: Multi-port EM subcircuit populated with lumped-element components from the vendor library and parameterized single pole, 8-throw switches for EM/circuit co-design

A standard script is available to create a schematic symbol based on physical layout details of the structure, helping engineers manage port connections for structures with many ports. This visual aid helps designers insert circuit components in their correct location on the board. In this example, an ideal switch with parameterized switch states was implemented in AWR Microwave Office software. This allows the designer to toggle through different impedance matching networks by adjusting the switch position, shown in Figure 15.

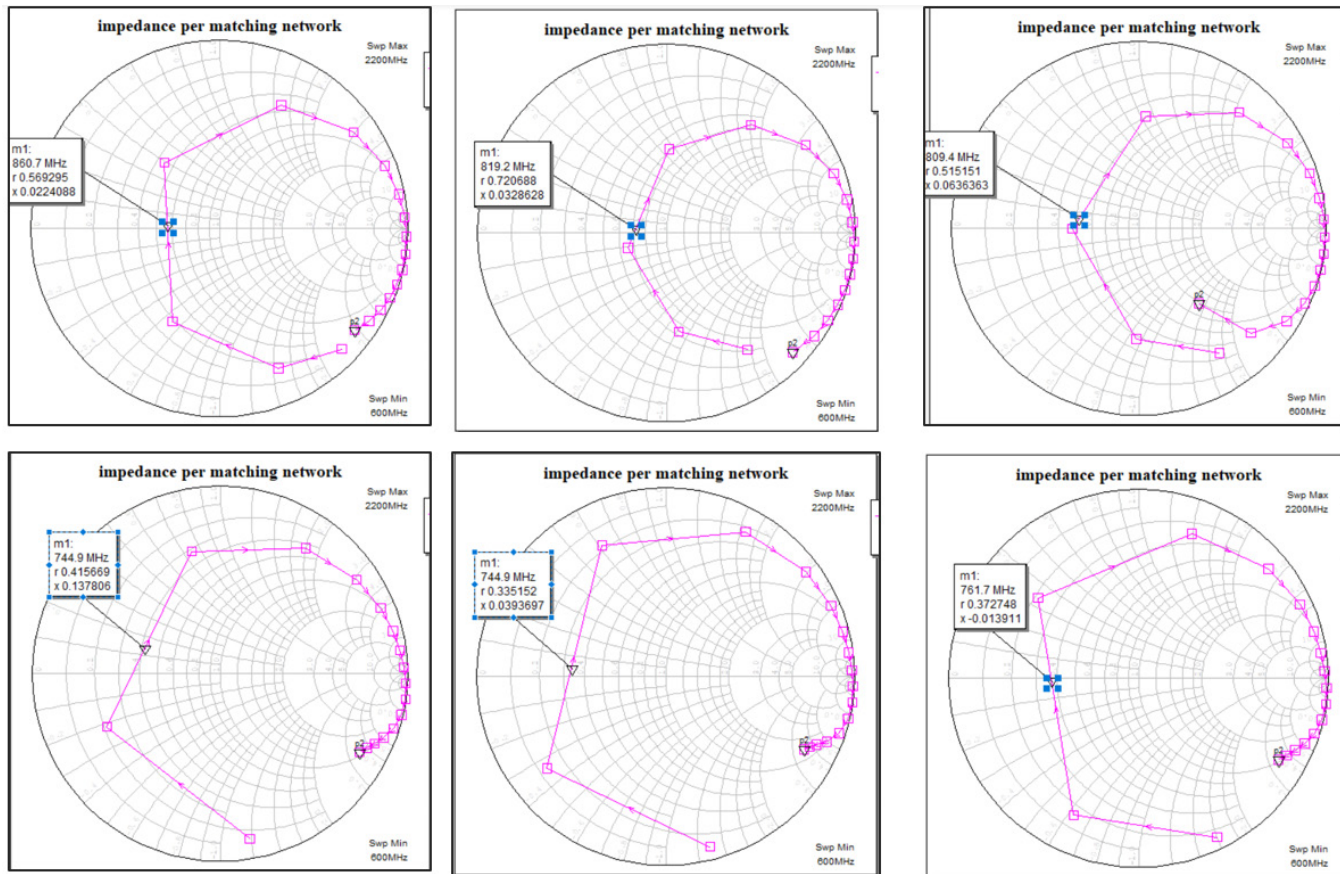


Figure 15: Input impedance (S11) vs. switch position looking into the matching network implemented on a four-layer cloT prototyping board terminated with the Fractus Virtual Antenna

This antenna manufacturer also supplies measured antenna gain information, which could be used by the antenna model in AWR VSS software as part of a link budget analysis when defining component specifications and validating system designs based on presumed path losses, receiver sensitivity, and regulated transmitter power levels (or effective isotropic radiated power [EIRP]).

Furthermore, AWR VSS software offers several preconfigured NB-IoT testbenches that allow the designer to examine various figures of merit including the modulated spectrum, the IQ constellation of the transmitted and demodulated signals, bit or block error rates, and throughput (Figure 16). By replacing the default device under test in this project with a single component or an entire RF link including the antenna and perhaps channel modeling of the propagation losses. The AWR VSS software's NB-IoT testbench lets engineers sweep various parameters, such as input power, or toggle different NB-IoT subcarrier modulation schemes ($\pi/2$ BPSK or $\pi/4$ QPSK) to investigate the impact on performance, such as error vector magnitude (EVM).

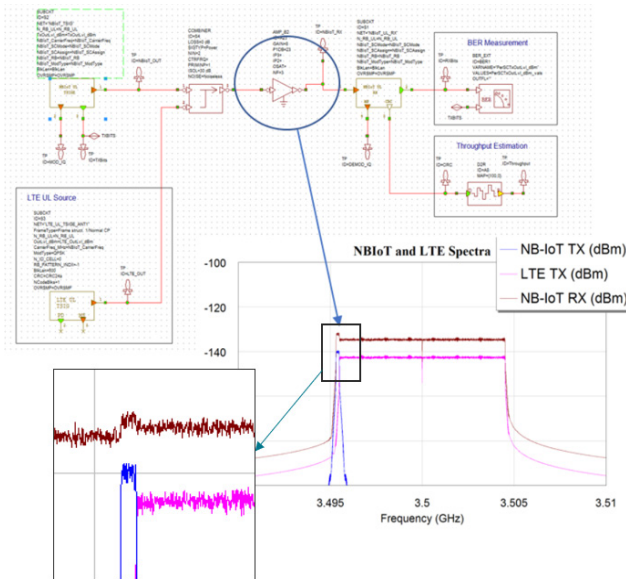


Figure 16: NB-IoT uplink to eNB RX testbench in AWR VSS software

With the RF design, analysis, and verification complete and EM, circuit, and system-level performance criteria met, the RF IP can be passed along to the layout team for any additional design integration, design rule check (DRC)/layout vs. schematic (LVS) and final signoff. To address the manufacturing flow, layouts from AWR Microwave Office software can be exported as a drawing interchange format (DXF) file (as well as GDSII and Gerber), which can then be imported into Cadence Allegro® PCB Designer for any further development (Figure 17).

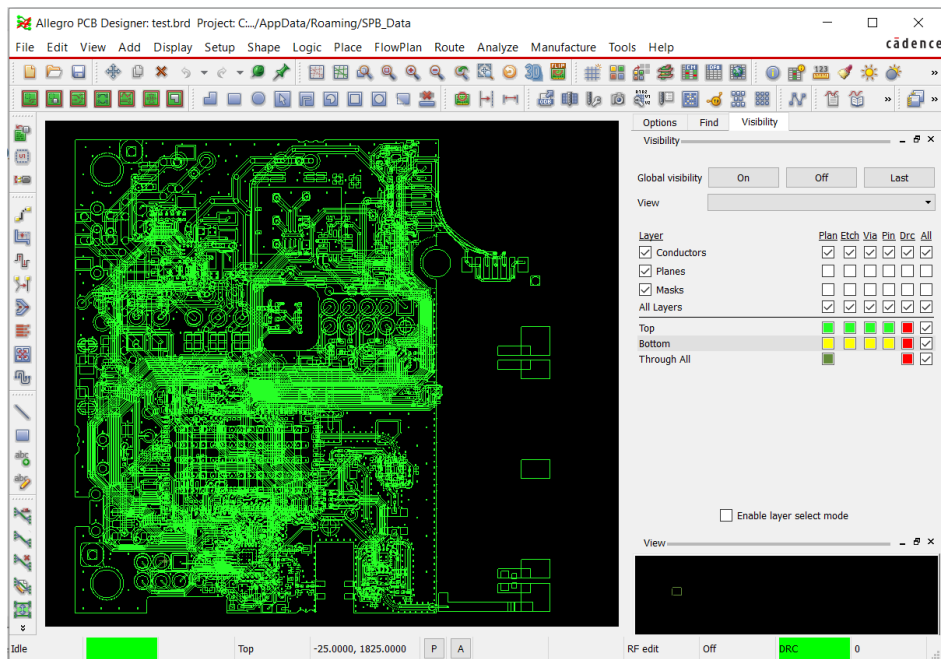


Figure 17: Complete cIoT board imported into Allegro PCB Designer from AWR Design Environment DXF export

Sub-6GHz Design for eMBB

For eMBB, the 3.4GHz-4.2GHz frequency range, also referred to as C-band, will aid the transition from 4G to 5G by providing access to a range of frequencies with less challenging propagation conditions and loss than occurs at mmWave. C-band supports transmission in a non-line-of-sight (NLOS) environment, facilitating indoor penetration on par with lower-frequency bands. Compared to mmWave, the benefits of C-band are both economic and technical:

- ▶ Overlaying C-band on top of existing macro-cellular or small-cell grids eliminates the need for new cell sites, unlike those required for mmWave.
- ▶ Access to a range of spectrum with fewer challenging propagation conditions than mmWave. This approach reinforces transmission in a NLOS environment and facilitates indoor penetration on a scale like lower-frequency bands.

C-band also uses time-division-duplex LTE technology (TDD-LTE), allowing transmission and reception on the same channel, compared to frequency-division-duplex LTE (FDD-LTE), which uses paired spectrum with different frequencies and a guard band. For a TDD-LTE device, this capability eliminates the use of a dedicated diplexer to isolate transmission and receptions, thereby reducing BOM costs.

At C-band, downlink coverage is greater than uplink coverage. This is due to the much larger transmit power of the gNodeB compared to the uplink transmit power of the user equipment (UE), as well as differences in uplink and downlink time-slot allocations. The application of beamforming technology reduces downlink interference and further increases the gap between C-band uplink and downlink coverage.

Simulations have shown that 5G radio base stations operating at 3.5GHz combined with advanced antenna techniques such as MIMO and beamforming can provide the same downlink coverage currently available with LTE 1800MHz. This allows the existing cell grid to be reused for the initial sub-6GHz 5G rollout. However, larger MIMO and beamforming arrays are not practical within the limited real estate of a handset. Therefore, if the uplink used the same frequencies as the downlink, the size of the cell would shrink to the maximum range in the uplink, limited by UE power and antenna gain.

Taking the downlink 50Mbps and the uplink 5Mbps as an example, the C-band uplink and downlink coverage differs by 16.2dB. While the C-Band downlink can achieve the similar coverage as the LTE 1800MHz, there is limitation in the uplink coverage which becomes a 5G deployment bottleneck negatively affecting the user experience. The difference between C-Band and LTE 1800MHz uplink coverage is 7.6dB for 2R and 10.4dB for 4R, as shown in Figure 18.

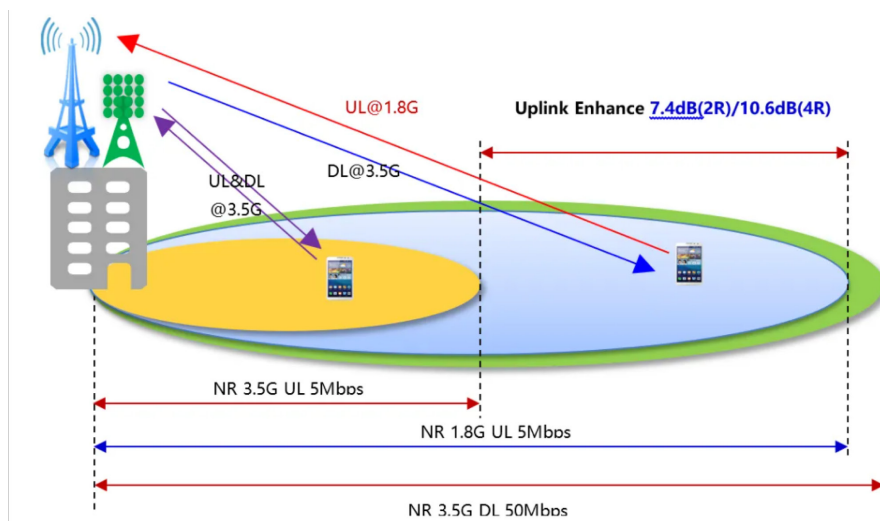


Figure 18: Downlink (50Mbps) and uplink (5Mbps) coverage at 3.5GHz and 1.8GHz (image courtesy of www.gsma.com)

Third Generation Partnership Project (3GPP) Release 15 introduced New Radio (NR) carrier aggregation (CA) and supplementary uplink (SUL) to handle the limited uplink coverage on the higher bands. These mechanisms rely on idle sub-3GHz band resources to improve C-band uplink coverage and enable 5G services to a wider area. These solutions drive the performance requirements of both base station and mobile device PA, RF front-end, and antenna technologies. Depending on the equipment being developed, designers must determine the individual component specifications based on the link budget. The electrical requirements, along with costs and size considerations, play a role in guiding the choice of semiconductor/integration technology best suited for the target application.

Link budgets are used to predict the received power in a communication system, which is ultimately limited by the achievable signal-to-noise ratio (SNR) at the receiver. The received power, in turn, is governed by channel losses and the transmitter's effective radiated isotropic power (EIRP), which is equal to the transmit power multiplied by antenna gain. Figure 19 shows the relationship between EIRP, number of antenna elements, available amplifier power at 1dB compression, and dominant semiconductor technologies. Gallium nitride (GaN) and gallium arsenide (GaAs) are the preferred semiconductors in front ends with arrays <100 elements and P1dB >20dBm, which is why III-V technologies are widely used in UE.

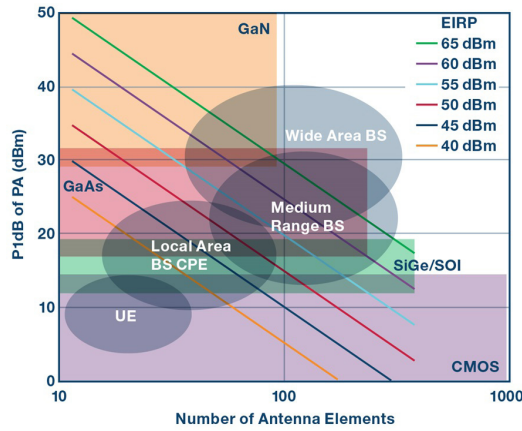


Figure 19: Amplifier output power (P1dB) for different semiconductor technologies vs. number of antenna array elements to achieve target EIRP values (image courtesy of Analog Devices)

For amplifiers designed as either discrete GaAs/GaN transistors on a PCB or as an integrated MMIC, the AWR Design Environment platform offers system, circuit, and EM co-design, supporting all phases of PA development. AWR software provides concurrent schematic and layout design entry and management while the AWR APLAC® HB Simulator's harmonic balance (HB) engine in AWR Microwave Office software offers rigorous frequency domain simulations of nonlinear RF networks.

Amplifier designs start with selection of an appropriate active device for the targeted frequency and performance targets, followed by the development of the bias and impedance-matching circuitry. Biasing and load/source terminations have a strong influence over amplifier performance, hence design aids in AWR software such as DC IV curve generation, load-pull analysis, and impedance-matching network synthesis play a supporting role in accelerating early design activity (Figure 20).

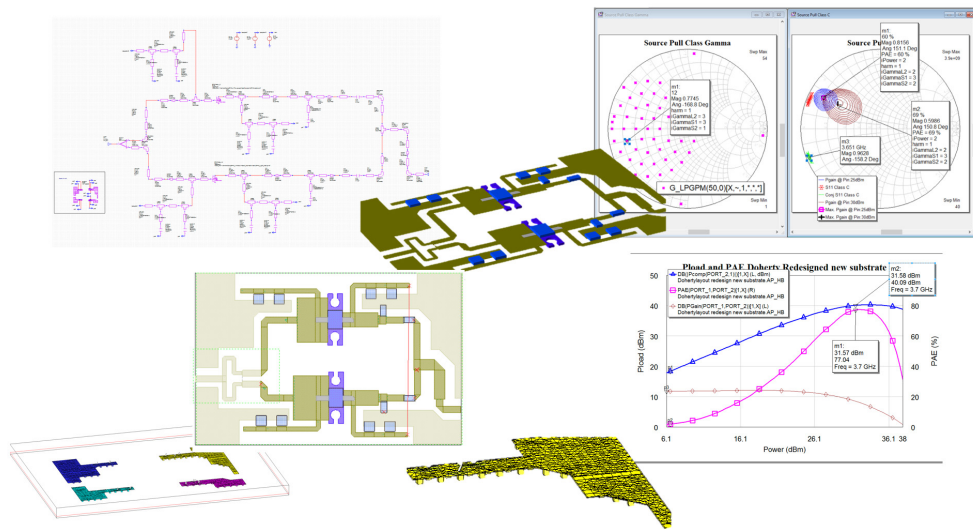


Figure 20: 3.5GHz GaN high-electron mobility transistor (HEMT) Doherty PA for 5G C-band base stations, designed with AWR software

The HB solver in AWR Microwave Office software verifies amplifier performance with specialized measurements such as noise figure (NF) and small-signal transmission and reflection parameters (S-parameters), as well as the nonlinear power, gain compression, and efficiency response to large-signal stimuli. In addition, the AWR APLAC HB Simulator supports circuit envelope analysis for circuits sourced with digitally modulated signals, providing simulation of key linearity metrics such as adjacent channel power ratio (ACPR) and EVM.

The 5G NR library option in AWR VSS software offers easy-to-configure signal sources and receivers that can be used to evaluate RF components and/or RF links using system-level measurements (Figure 21). Testbenches with preconfigured 5G NR TX and RX blocks and measurements support analysis of networks with flexible signal configurations with variable signal power, carrier frequency, modulation and coding scheme (MCS), bandwidth, and subcarrier spacing. These testbenches are used to validate if a front-end design meets the requirements defined in the 3GPP specifications for sub-6GHz (FR1,) as well as mmWave (FR2) bands.

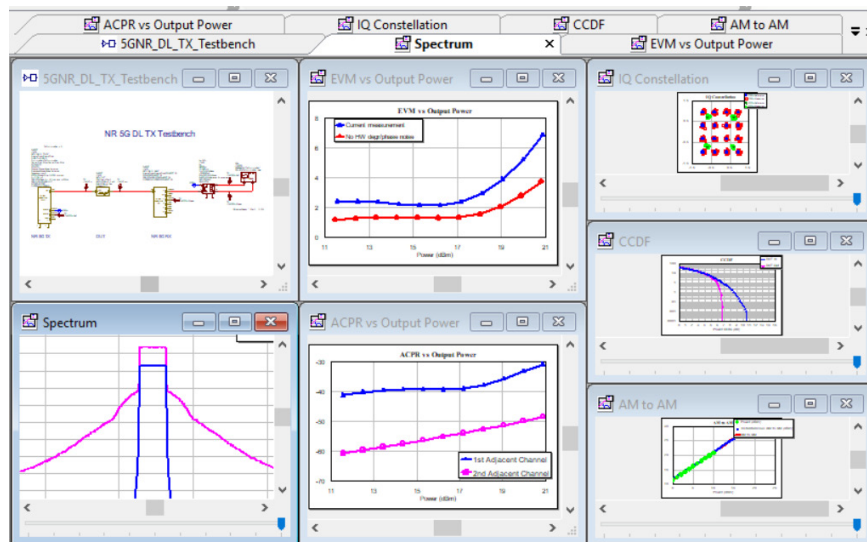


Figure 21: ACPR, EVM, complementary cumulative distribution function (CCDF) measurements performed in the AWR VSS software's 5G NR library option

Because 5G communications is developing rapidly, early delivery of products to market is critical. For engineers at Mitsubishi Electric, the integrated AWR software platform enabled fast development of their 28GHz GaN PA MMIC, while meeting all their technical requirements (Figure 22). Throughout the design process, EM analysis was used for passive component and interconnect modeling and optimization. The AWR AXIEM analysis was used to verify the behavior of the Doherty PA's critical impedance matching/inverting network and output combiner prior to tapeout. In addition, ready access to a design kit for the Mitsubishi Electric GaN process reduced product development time by 50%.

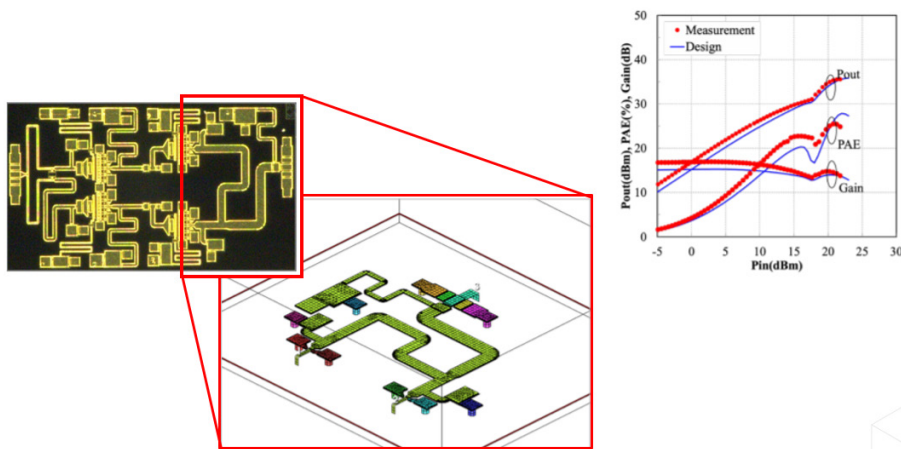


Figure 22: 28GHz GaN Doherty PA combiner network analyzed with the AWR AXIEM analysis

EM analysis and design optimization are carried out at the component and subcircuit level to ensure that parasitics and any inadvertent EM coupling between structures is incorporated into the simulation. Towards the end of the design phase, the Cadence Clarity™ 3D Solver addresses critical interconnect modeling of large-scale, integrated RF/mixed-signal electronic systems. Cadence's industry-leading distributed multiprocessing technology enables the solver to deliver virtually unlimited capacity and 10X speed, which are required to efficiently and effectively address these larger and more complex structures. The Clarity 3D Solver eliminates the need to subdivide structures into smaller sections, which is often necessary to accommodate the capacity limits common among legacy 3DEM simulators.

mmWave Chip, Package, and Board Beamforming Solutions

5G data rates exceeding 1GB/s will be supported by the available bandwidth at mmWave spectrum and use of beam steering phased array antennas and multiple communication chains, which can range from eight to 64 elements in a typical system. A reference design has been developed to demonstrate how software tools from Cadence support the development of such a system from the 5G antenna array on a PCB through the package-on-package design and complementary metal-oxide semiconductor (CMOS) receiver IC, shown in Figure 23.

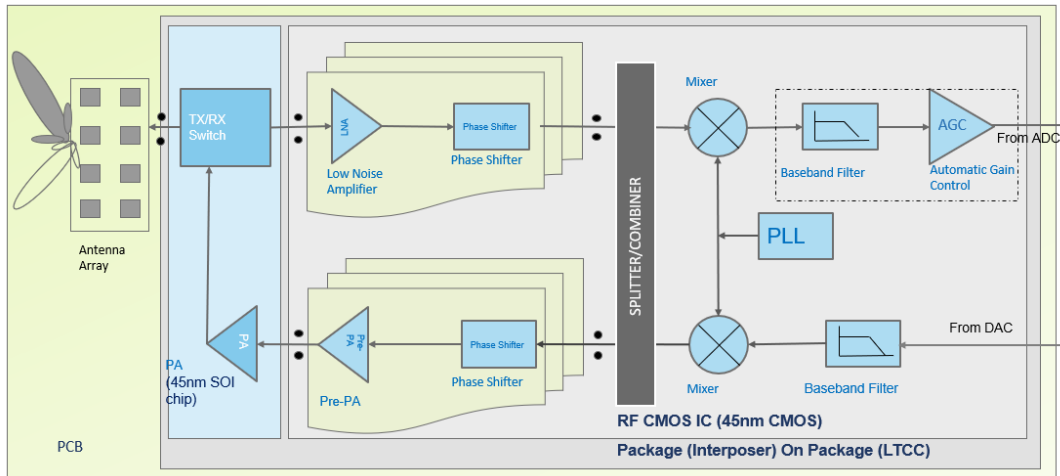
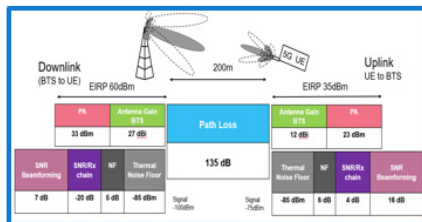


Figure 23: 5G RF beamformer for an eight-element receiver

The reference design has been developed with a full range of Cadence solutions, including:

- ▶ AWR VSS software for budget analysis and component specification, phased array configuration, and simulation of digital modulation measurements such as ACPR, EVM, and BER.
- ▶ Virtuoso RF Solution and Spectre RF Option for design entry and simulation of the 45nm CMOS RFIC eight-channel receiver chip.
- ▶ Cadence EMX® Planar 3D Solver for analysis of on-chip passives and interconnects.
- ▶ AWR AXIEM analysis for analysis of PCB feed structure and eight-element (4x2) antenna array
- ▶ Allegro PCB Designer for physical layout design
- ▶ AWR Microwave Office software for III-V and off-silicon circuit design

System designs often start with budget analysis used to define the RF link, calculate the cascaded performance of the RF link, and determine individual component specifications. The reference design began with back-of-the-envelope approximations taken from published literature, including likely component block performance based on historical results for the target IC process, system requirements (data rates and coverage range), channel losses, allowable transmitter EIRP, and receiver sensitivity (Figure 24).



200m link at 28GHz	Downlink	Uplink
	(Tx)	(Tx)
Total Transmitted Radiated PA power (dBm)	33	23
Antenna Gain (dBi), G_{array} Tx/Rx	27	12
Transmitted Eff. Iso. Rad. Power (EIRP) (dBm)	60	35
Path Loss (dB)	135	135
Received Power (dBm)	(Rx)	(Rx)
	-100	-75
Thermal noise floor (dBm) for 850MHz BW (BW_{sig})	-85	-85
RX Noise Figure, NF_{Rx} (dB)	5	6
SNR per RX element (dB)	-20	4
RX Antenna Gain (dB)	27	12
RX SNR after beamforming, SNR_{sig} (dB)	7	16

Figure 24: Proposed downlink/uplink budget (power, gain, NF) for 200m link at 28GHz

In this case, the thermal noise floor for a 400MHz bandwidth is calculated to be -85dBm, assuming the receiver has a cascaded NF of 6dB that increases the noise floor to -79dBm, which requires a signal strength of at least -75dBm (per antenna element) to achieve a minimum signal-to-noise ratio (SNR) of 4db. To obtain that received power level (-75dBm), working back towards the transmitter through a line of sight path loss of 135dB requires an EIRP of 60dBm, which translates into an output power of 33dBm (2w) from the base station PA for an antenna with 27dB of gain.

AWR VSS software was used to characterize the receiver chain with behavioral models, performing budget analysis to obtain the overall cascaded figures of merit and spur heritage to examine the impact of nonlinearities on generating unwanted tones in the system. These analyses helped guide early design decisions such as P1dB and IP3 considerations to reduce unwanted harmonics from device nonlinearities, as well as filtering to mitigate interference. Furthermore, AWR VSS software can perform time-domain analyses from the same schematic to investigate BER, IQ constellation plots, and spectral regrowth, as shown in Figure 25.

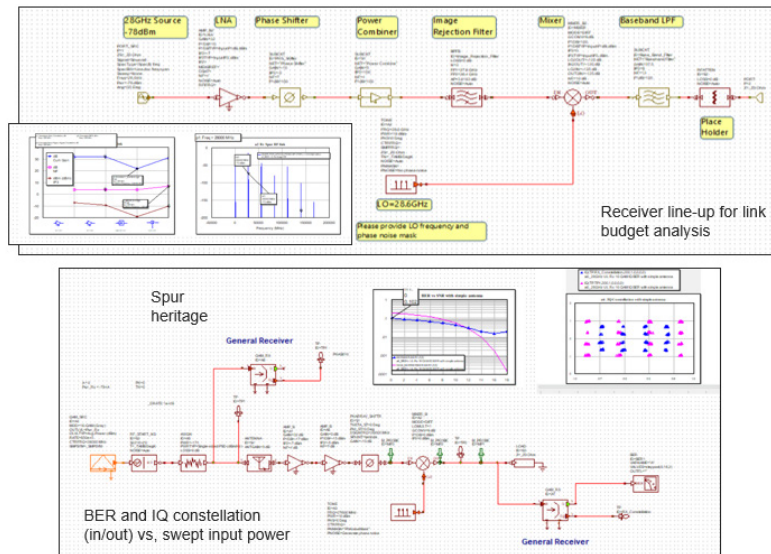


Figure 25: Single channel link in AWR VSS software based on component blocks using behavioral models with parameters derived from early Virtuoso RF Solution/Spectre RF Option simulations

After obtaining the desired channel link budget response, attention can be turned to developing the individual RF front-end blocks at the circuit (transistor) level with layout and construction of the eight-channel receiver in both AWR VSS software and the Virtuoso RF Solution (Figure 26). The RFIC was designed in Virtuoso RF Solution using a generic process design kit (PDK) based on 45nm CMOS technology and simulated using the HB engine available in Spectre RF Option. The EMX Planar 3D Solver was used to extract the broadband response of the on-chip passive components and interconnects.

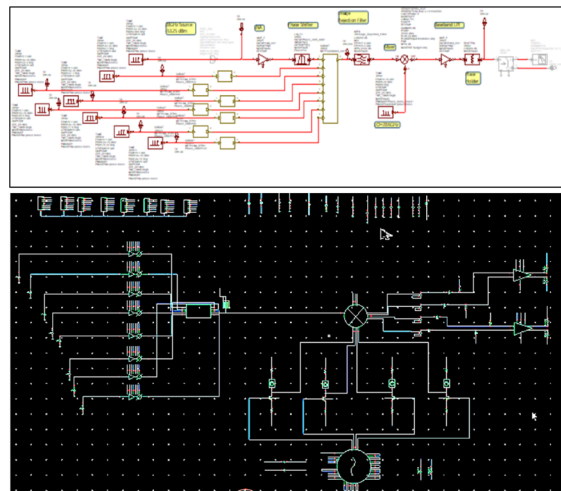


Figure 26: The eight-channel receiver RFIC modeled in AWR VSS software with behavioral models (top) and top-level schematic in Virtuoso RF Solution (bottom)

The post-layout Spectre RF Option simulation results were then used to create data files (S-parameter, phase noise mask, spur table, or am/am-am/pm) in AWR VSS software to provide a greater level of detail defining the behavior of the various blocks, thereby increasing the accuracy of the simulation. The schematic, layout, and post-layout simulation results for the individual component blocks are displayed in Table 2.

Virtuoso Design	LNA	Phase Shifter	Combiner	Mixer
Schematic				
Layout				
Response				

Table 2: 28GHz receiver component blocks implemented in Virtuoso RF Solution

The next phase of the design focuses on the heterogeneous integration of the RFIC into the packages and development of the PCB with an embedded 2x4 patch antenna array. To implement the packaging, the RFIC design (parasitic-aware schematic) was exported to a SiP as a simple footprint for place and route operations using the schematic-to-SiP layout feature from the RF module pull-down menu in the Virtuoso Schematic Editor. The next step was to bind this footprint to the original IC schematic symbol or sub-circuit. This is the same symbol that the IC designer has been using in the top-level IC simulations. The Virtuoso System Design Platform provides an intelligent mapping mechanism to create a 1:1 map between the footprint terminals and the IC symbol terminals (Figure 27).

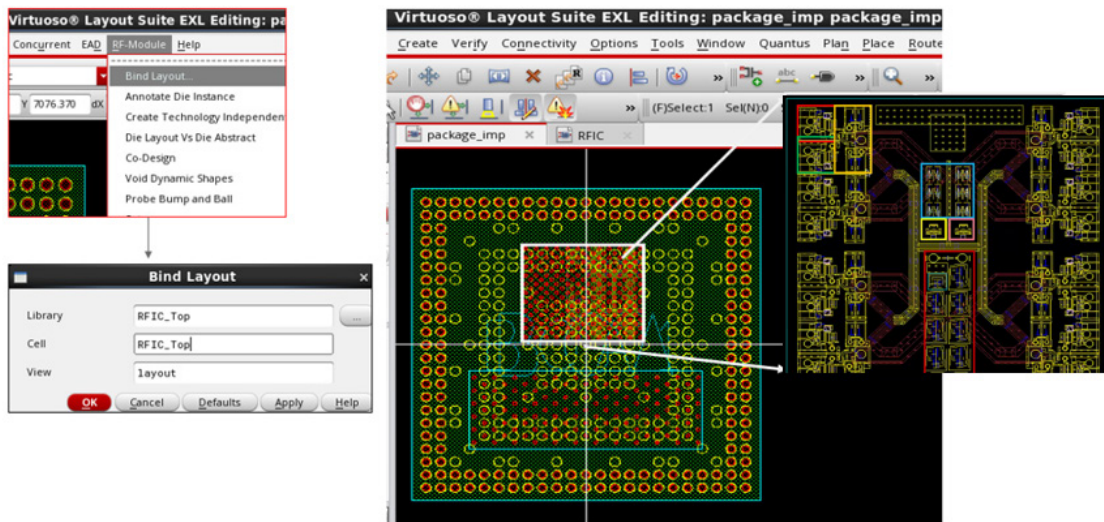


Figure 27: The Virtuoso System Design Platform allows users to bind the RFIC footprints in the package layout to the actual RFIC layout cell view

Package-aware RFIC simulation can then be performed based on EM extraction of critical nets from the package design layout. Specific to this design, the Clarity 3D Solver can be used to extract the interconnects between the individual RFIC receiver channels through the package routing to each element of the patch antenna array on the PCB. To focus strictly on the PCB feed and antenna array response, the board layout was imported into the AWR Design Environment platform through the IPC-2581 file format for EM analysis with the AWR AXIEM analysis. In addition to S-parameter extraction, AWR AXIEM analysis can provide surface currents and radiation plots of the individual patch antennas or the entire array (Figure 28).

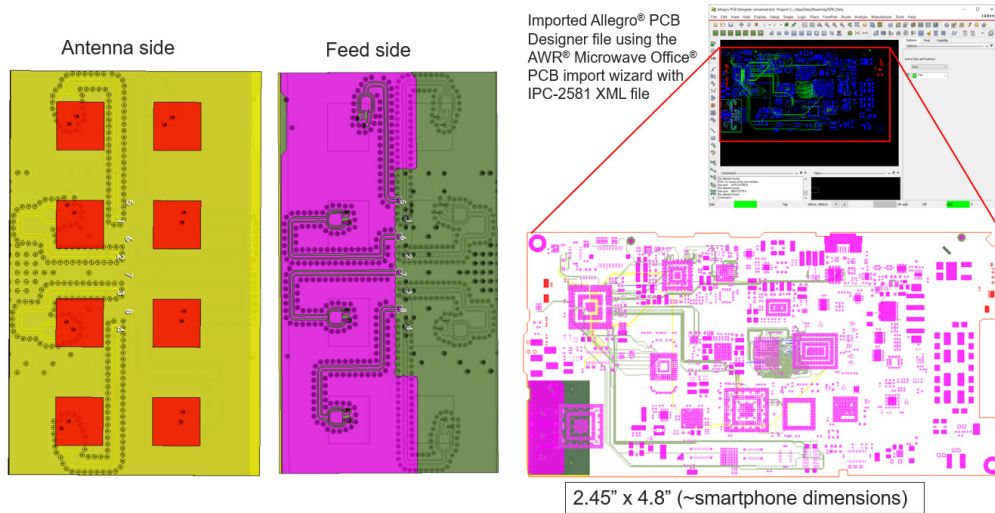


Figure 28. 5G PCB imported into the AWR Design Environment platform for EM analysis of 2x4 antenna array

In addition to EM analysis of the initial array, the designers used the phased array generator wizard in AWR VSS software to rapidly configure the physical array, assign antenna radiation patterns derived from AWR AXIEM analysis for the individual patch antennas, and model mutual coupling and edge/corner behavior. The wizard also allows designers to specify link and feed performance, incorporate gain tapering to reduce antenna side lobes, and investigate the impact of element failures on the overall array performance. It provides real-time visualization of far-field radiation patterns from all these user-specified parameters and then automatically generates either a system or circuit-based network in AWR Microwave Office software for further development and EM/circuit analysis of the complete array, as shown in Figure 29. The resulting array can also be incorporated into the receiver design link.

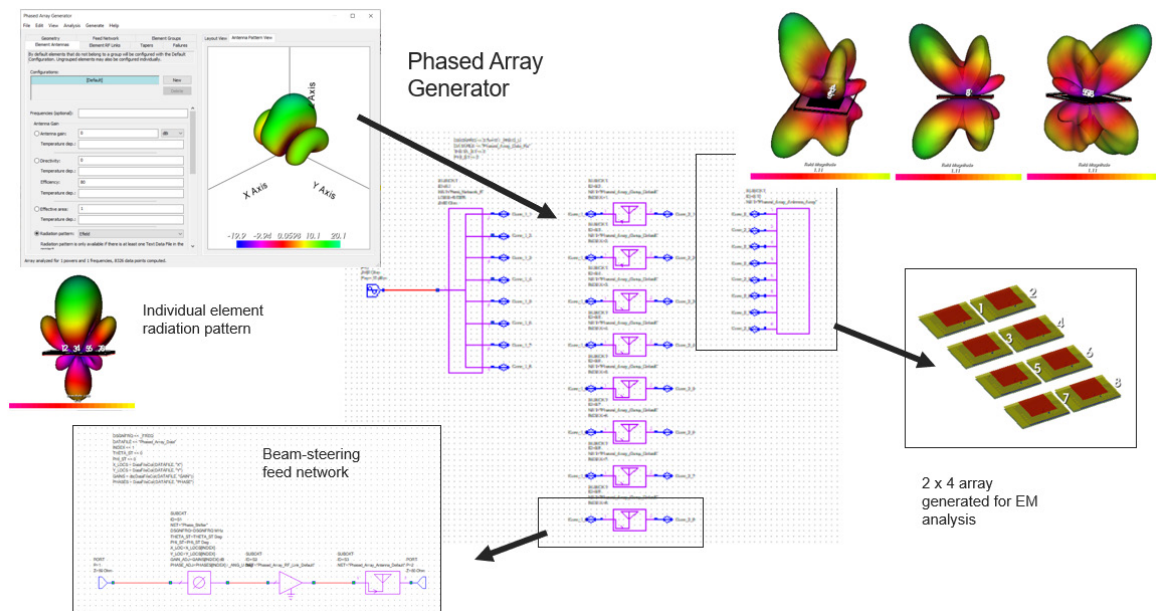


Figure 29. The phased array generator wizard in AWR VSS software creates a user-configured array structure and feed networks for RF front-end design and implementation

Conclusion

Next-generation communication systems targeting 5G/6G functionality will provide massive connectivity to the internet with extreme capacity, coverage, reliability, and ultra-low latency, enabling a wide range of new services and business opportunities. The anticipated performance will be made possible through a range of innovative technologies, implemented through complex RF front-end architectures and highly integrated multi-fabric electronics. RF to mmWave design and multi-fabric design and manufacturing software will be critical to the development of these technologies.

To power the technologies and products that will realize 5G/6G performance across chips, IP, packages, and PCBs, Cadence has developed the Intelligent System Design strategy for delivering its world-class computational software capabilities across all aspects of the design of electronic systems. This white paper has presented several examples of how Cadence is uniquely positioned with deep expertise and pivotal leadership in computational software, along with the broadest, most integrated design solution, to bring the Intelligent System Design strategy to the communication products of the future.



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