Power Envelope Tracking for Mobile Power Amplifiers

Have you heard the story about the guy who had to recharge his 4G phone twice a day? Unfortunately, he was not happy with his phone.

This story has been happening as the demand for high-speed data increases and battery capacity has not matched advances with communications technology. It’s not the battery at fault but the technology needed to power the amplifier on the phone. For years, normal DC-DC converters managed the battery power flowing in the phone to different chips. This included the power amplifier (PA) for driving the cellular signal back to the base station, which worked fine when the peak-to-average power ratio (PAPR) was relatively small for 2G and 3G signals. As the technology has progressed from GSM to GPRS to WCDMA to HSPA, the PAPR has increased progressively. Now LTE or 4G has a much higher PAPR that impacts the draw of power from the phone. In Figure 1 you can see this progression of technology for a typical PA output based on a given power input from a device battery.

![Figure 1. The Evolution of PAPR for Different Wireless Standards: The chart displays power in from the battery (Pin) versus power out (Pout) for a typical PA. Power compression of signals can vary depending on the PA design but the PAPR is consistent.](image)

The DC-DC converter pulls power from the device battery at a linear level at the peak of the signal power, which is not efficient. A better way to draw power is to anticipate the peaks of the cellular signal and supply only the needed power to the PA. This method of providing power is called power envelope tracking (ET). See Figure 2 for the ET method.
In the past decade, power ET technology has solved this dilemma for base stations to not only save power but also prevent overheating because the PAs deal with power on the order of 200 W or higher. Now semiconductor technology has reached a point where DC-DC converters are available for mobile devices that can provide the needed modulated power to the PA, which is timely because 4G technology like LTE is forcing better efficiencies from PAs. Now how do you test this new technology? Here’s an outline of this process working from a PA test solution.

Challenges Performing ET Test

ET test adds complexity to yet an already complex system. The first challenge with ET is generating the modulated power supply, which can require up to 2 W and tens of megahertz of bandwidth. This is an uncommon specification for a power supply so many PA manufacturers use a DC-DC converter that has been modified to perform the power modulation. These chips take as input a DC power supply and the envelope waveform used to control the amplifier’s gain, as well as some digital lines to control the chip. The output is a high-power, modulated waveform that powers the amplifier under test. See Figure 3 for a typical RF PA test setup that has been expanded to support ET.

Figure 3. This is a typical configuration for an RF PA test with ET capability.
The major challenge from a test and characterization perspective is synchronizing the different instruments necessary to perform ET. Most importantly, the RF signal generator and the baseband arbitrary waveform generator (AWG) must be synchronized with minimal jitter. Furthermore, it must be possible to skew the delay of the baseband envelope relative to the RF waveform with sub-nanosecond precision. Achieving this level of synchronization with traditional benchtop instrumentation can be difficult and most likely involves integrating hardware from a variety of vendors, complicating the application software.

National Instruments makes this process as straightforward as possible by simplifying the synchronization challenges and consolidating the hardware and software into a single platform. The PXI backplane (see Figure 4) routes all clock and trigger lines necessary for synchronization within the chassis, eliminating the need for an external clock and trigger routing network. To achieve sub-nanosecond levels of synchronization and repeatability, NI-TClk is used to coordinate the clock and trigger distribution among multiple modular instruments. For more information about how NI-TClk can synchronize multiple instruments with jitter as low as 20ps, read National Instruments T-Clock Technology for Timing and Synchronization of Modular Instruments.

Finally, NI’s diverse modular instrumentation product offerings can address every component of an ET capable RF PA test setup. You can consolidate a full PA test system into a single PXI chassis and a uniform collection of hardware driver APIs, which simplifies system integration and test development.

**NI Test Solution**

**Hardware Setup**

To modify a standard PA test solution to accommodate ET testing, you must add an AWG to the system (see Figure 3). The AWG must be capable of driving both single-ended and differential loads, applying common mode and differential DC offsets, variable gain settings, as well as flexible clocking options. The NI PXIe-5451 is a 400 MS/s 2-channel AWG that meets all of these requirements. It also features a number of onboard signal processing functions, including finite impulse response (FIR) filtering for pulse shaping and interpolation, flatness correction, and a digital upconverter that can reduce software preprocessing. Learn more about the NI PXIe-5451.
The RF signal generator used for this application is the 6.6 GHz NI PXIe-5673E vector signal generator (VSG), which has over 100 MHz of bandwidth. The NI PXIe-5673E is composed of three separate modules: the NI PXIe-5450 arbitrary waveform generator, NI PXIe-5652 local oscillator, and NI PXIe-5611 I/Q vector modulator.

![Image of the front of the NI PXIe-5673E VSG showing three separate modules.](image)

**Figure 5.** The front of the NI PXIe-5673E VSG shows three separate modules.

See Figure 6 for the setup used to verify synchronization and repeatability of the VSG and AWG. An NI PXIe-5673E VSG generates the RF waveform and the NI PXIe-5451 generates the baseband envelope waveform. An NI PXIe-5154 1 GHz digitizer verifies synchronization, but you can use any scope with a sufficiently high sample rate and bandwidth.

![Image of the test setup verifying synchronization.](image)

**Figure 6.** This test setup verifies that the AWG and VSG are synchronized.

To synchronize the AWG and VSG, both devices must share the same 10 MHz reference clock. The reference clock can be sourced by the PXI 10 MHz backplane clock, one of the instruments, or an externally supplied 10 MHz clock.
**Software**

In Figure 7 you can see an overview of the software steps necessary to produce the RF and envelope waveforms necessary for ET. The LTE waveform to be generated is created using the NI LTE Toolkit, or read from a file. The envelope waveform, which is a function of the LTE waveform, is then calculated. You may also want to perform some additional signal processing, such as digital predistortion or other filtering operations to optimize the waveforms for ET. The VSG is configured to generate the LTE waveform and the NI PXIe-5451 is configured similarly to the NI PXIe-5450 AWG in the NI PXIe-5673E VSG (see Figure 5). The envelope waveform is then time shifted relative to the RF waveform and written to onboard memory, along with hardware scripts used to control waveform generation. (See the next section on Waveform Generation Delay Implementation for the algorithm used to time shift the envelope waveform.) Finally, the devices are synchronized using TClk and initiated.

![Diagram](image)

**Figure 7.** This overview shows the software process for generating the RF and envelope waveforms necessary for ET.

The software necessary to synchronize the baseband envelope generator with the RF signal generator is relatively simple. Once the VSG and AWG share the same reference clock, NI-TClk is used to synchronize the sessions. At this point, the waveforms generated by the AWG and VSG are phase-locked with a repeatable delay between them. This delay comes from the analog path between the NI PXIe-5450 AWG through the NI PXIe-5611 I/Q modulator that NI-TClk does not account for (see Figure 5). Because this delay is constant, you can remove it by delaying the AWG relative to the VSG. For many ET applications the ability to delay the AWG relative to VSG, or vice versa, is crucial to find the delay that maximizes the device performance. The delay must be repeatable with minimal jitter because skewing the delay by only a few nanoseconds from the optimal value can affect device linearity by several dB.

**Waveform Generation Delay Implementation**

Remember that the ability to control the delay between the VSG and AWG is crucial to ET chip test and characterization. The delay can be implemented either in hardware by adding wait samples and skewing sample clocks or in software with DSP. Although it is possible to implement the delays in hardware, it requires the ET waveforms to be resampled to 200 MHz to specify a delay with nanosecond resolution. Resampling the waveform may not be an option for some customers so the software implementation is preferred.
The software delay algorithm uses the discrete Fourier transform (DFT) time-shifting theorem, which states that delaying a periodic time-domain waveform by \( n_d \) samples modifies its DFT representation by the factor \( e^{-(j2\pi k/N)n_d} \), where \( k \) is the discrete frequency index.

You can use this result to delay \( x[n] \) by \( n_d \) samples by performing the following steps:

1. Take the \( N \)-point DFT of \( x[n] \) to get \( X[k] \), \( 0 \leq k \leq N - 1 \)
2. Multiply \( X[k] \) by \( e^{-(j2\pi k/N)n_d} \), \( 0 \leq k \leq N - 1 \)
3. Take the inverse DFT of the resulting transform

**Results**

Sample code that synchronizes the waveforms and allows the user to delay one relative to the other with picosecond resolution is available in both NI LabVIEW system design software and ANSI C. You can find sample projects at the end of this article. Figure 8 displays typical results of the LabVIEW sample code using an NI PXIe-5154 1 GHz digitizer to sample the data. In this example, the baseband envelope signal is simply a scaled version of the magnitude of the LTE waveform. A quick visual inspection reveals that the baseband envelope tracks the RF waveform.

![Figure 8: RF LTE Waveform With Baseband Envelope](image)

Figure 9 shows the front panel of the LabVIEW ET demo. Aside from some standard hardware resource controls, a few other parameters are worth describing. First, is the *Waveform IQ Rate*. This demo assumes that the RF and envelope waveforms are both sampled at this same rate, which can be any value. As discussed earlier, to delay the envelope and RF waveforms by an arbitrary amount both waveforms are resampled to 200 MHz. The second important parameter is the control *AWG Delay Relative to VSG*. This is the control that actually delays the envelope relative to the RF waveform, or vice versa, by entering a negative delay.

Looking at the RF and envelope waveforms themselves, as in Figure 8, it is difficult to confirm with nanosecond precision that the waveforms are being delayed as expected. The waveform graph in Figure 9 displays digitized marker events that were exported on the first sample of the RF and envelope...
waveforms. Using cursors, you can see that the RF waveform is delayed by 7 ns relative to the envelope, which is predominantly due to path delays in the NI PXIe-5611 upconverter and cable length differences. To have the two waveforms to overlap exactly, the control \textit{AWG Delay Relative to VSG} should be set to 7 ns, as shown in Figure 10.

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig9.png}
\caption{Front Panel of the LabVIEW ET Demo: Marker events are exported from both the VSG and the AWG. Using cursors, you can see that the RF waveform is delayed by 7 ns relative to the AWG.}
\end{figure}

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{fig10.png}
\caption{The 7 ns delay between the RF waveform and the envelope waveform has been compensated for by delaying the AWG by 7 ns.}
\end{figure}

Considerable power is wasted when using conventional DC power supplies, making ET capability crucial for LTE power amplifiers. Though this technology promises to significantly improve PA efficiency, modifying existing test and characterization setups to accommodate ET is a difficult and costly endeavor. With the NI platform and the sample code provided with this article, you can retrofit an existing NI PXI power amplifier test station to support ET at a fraction of the cost and time required with conventional benchtop equipment.

To learn more about this ET test solution, contact Heath Noxon at heath.noxon@ni.com.