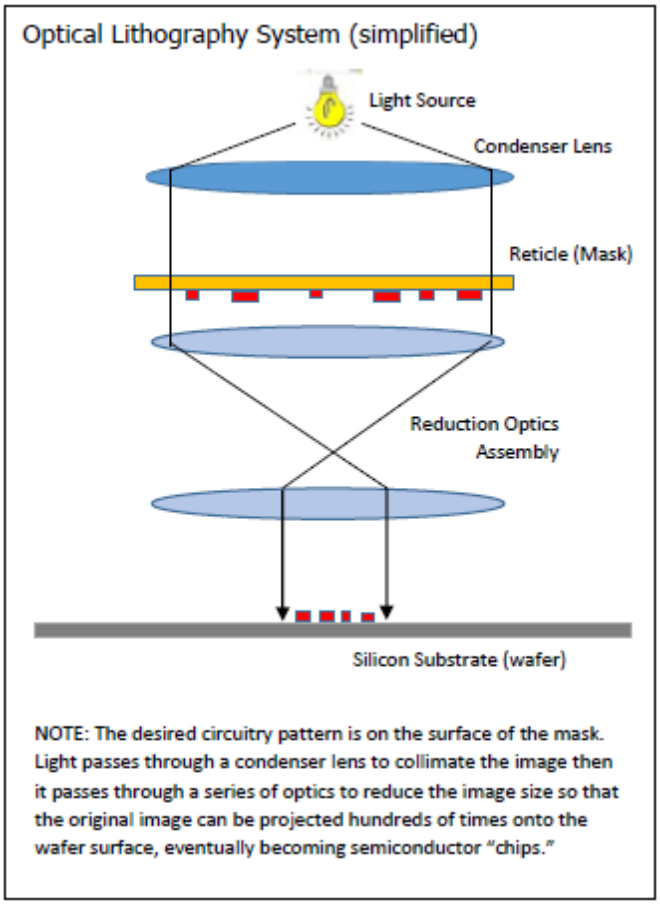
CMP: THE ENABLING TECHNOLOGY
Electronic Military & Defense, 2016

The digital world is exploding! In military and commercial applications, the highest levels of technology in use today are matched with a multitude of real, hands-on devices and sub-components within those devices that while not obvious to the casual observer, and perhaps not easily understandable to the average user, are integral to our everyday lives. In military, medical, automotive, banking, retail, home management, business, and pleasure, we use digital technologies without even thinking about them. They are here, we use them, and we go on with our lives. However, we are not talking about things that you can see. We are talking about things you cannot see, at least not without very high powered magnification.

The Digital Manufacturing Revolution

The enabling technology for all things digital is Chemical Mechanical Polishing for the Planarization of Thin Films on Semiconductor Circuitry, better known as "CMP." Understanding the minute technical details of the CMP process is perhaps not necessary in this discussion, but understanding why it is important in the manufacture of advanced circuits and digital devices will help buyers and users to make critical decisions related to the suppliers' value propositions related to robust design, extended useful life, compact structures, and Mean Time Between Failures (MTBF) all of which are made possible and then optimized by smaller and smaller design nodes (feature sizes), and multilayer structuring (made possible by the CMP process).



NOTE: The desired circuitry pattern is on the surface of the mask. Light passes through a condenser lens to collimate the image then it passes through a series of optics to reduce the image size so that the original image can be projected hundreds of times onto the wafer surface, eventually becoming semiconductor "chips."

In very early semiconductor manufacturing history, one layer of circuitry was placed on a silicon substrate by a process known as photolithography. This is a process similar to passing light through a "negative" to expose an image on photosensitive paper via an "enlarger." This process, or one very similar to it, is used to make the copper wires of the electronic circuit and to make interconnects for transistors, diodes, and capacitors (the "devices") through a process that projects light through a glass "mask" rather than a negative, and reduces the image of the circuit pattern rather than enlarging it.

As the market (meaning you and me) started to demand faster and faster devices, designers and manufacturers of the chips, started to make the wires and devices smaller and smaller, so that more and more of them could be placed on the available "real estate" of the silicon wafer surface. Major manufacturers like Fairchild, IBM, Motorola, Intel, Texas Instruments and others then started to build one layer of circuitry on top of another so that the devices could "talk" to each other faster and speed up computer capabilities. Each device layer (the metallization layer that is the electrical conducting portion) needs a layer of insulator on top of it (the common insulator is silicon dioxide – glass), to prevent "cross-talk" or "electro-migration" or as most of us know it as being a "short." When the insulator layer is applied it is very thin, perhaps just a few thousand Angstroms (a Helium atom has a theoretical diameter of one Angstrom) but it is also conformal, meaning that it takes the shape of whatever it is covering, be it a transistor, a diode, a capacitor, or a copper wire. In the early days, the common insulators were either "Spun-on-glass" or SOG, a liquefied silicon dioxide, or a thermal oxide.

So as the wires were getting smaller as were the individual devices, the layers of circuitry started to be multiplied in an attempt to make better use of the available surface area of the wafer, the "real estate." The conducting wires in those days were 0.5 microns and larger. Going smaller is where the challenges started.

Size Does Matter

The small copper wires in modern circuits by contrast are in the range of tens of nanometers.

What?	Typical Dimensions	In Nanometers (nm)
Sheet of paper (20#)	0.004 inches (or 0.1mm, or 100 microns)	100,000 nm
Human Hair	0.007 inches (or 0.017 to 0.180 mm, or 178 microns)	178,000 nm
Typical copper wire size in modern micro-circuitry	0.022 microns (or 0.000000886" or 8.7 billionths of an inch!) 0.014 microns (or 0.000000551" or 5.5 billionths of an inch!) 0.007 microns (or 0.000000276" or 2.7 billionths of an inch!)	22 nm (in production) 14 nm (early production) 7 nm (experimental)

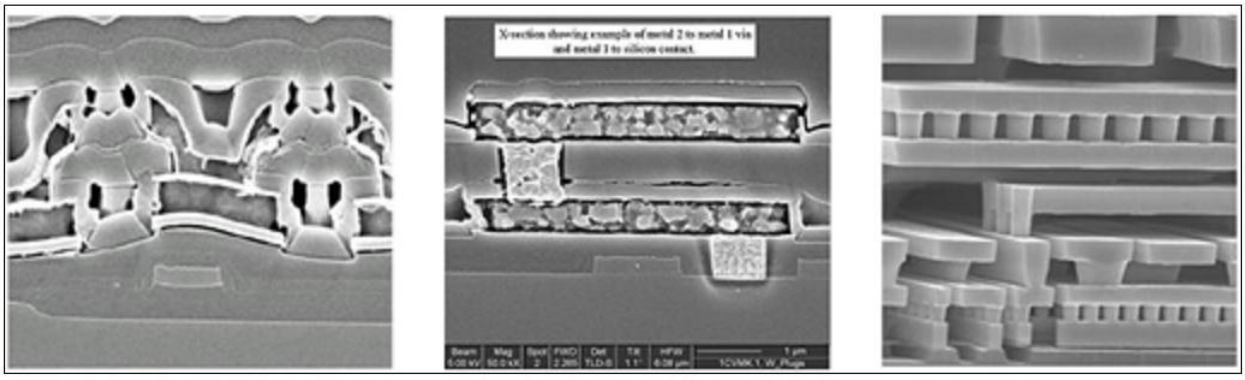
How small is a nanometer? You need a Scanning Electron Microscope (SEM) to even start to get a glimpse. Looking at it from one point of view, if a nanometer were as large as a millimeter, then a 12-inch ruler would be as large as a football field! Liberally stretching these numbers into one more example, these ridiculously small modern dimensions could mean that it is possible to place as many as 8,000 of these small 22nm copper wires across the diameter of a typical human hair!

But, I am getting way ahead of myself. To make these tiny features, it requires a photolithography system that has a very short focal length so that the system can focus down to the dimensions required to make nanometer (nm) sized structures. Using Chemical Vapor Deposition (CVD) techniques to deposit the various layers of insulator (silicon dioxide – glass) after each layer of metal circuitry, provides for a widely accepted means of

separating metal layer from metal layer with the glass layer in between. Tiny contact vias are etched in the proper places so that copper interconnects can be made to allow devices to interact through the length, width, and height of the many layers of circuitry. It is similar to a multi-story office building with stairwells and elevators so that people can go around the building and communicate not only through the length and width of their particular floor, but also from floor to floor.

The Challenge

When applied, however, the layer of silicon dioxide, (the insulator layer), is conformal. It replicates the shape of the devices that it is covering; it becomes topographical. The humps and bumps that are produced are often larger than the focal budget of the photolithography system that is going to be used later on to try to make another pattern of devices. This causes the photolithography system to be unable to focus properly, and simply put, a blurred image will appear instead of the crisp image so necessary at these tiny dimensions. The issue with blurred images was not a big concern back in the late 1970's and early 1980's when the copper, or tungsten, or aluminum wiring was 0.5 microns and larger (22 times larger than they are in production today) because acid etching (spin-etch back) techniques were good enough to planarize well enough to make for a flat enough surface for the succeeding insulator layers. However, when designers started to develop wiring smaller than 0.5 microns, it required a major change in manufacturing thinking.



Non-planarized layers (typical topography of pre-CMP manufacturing)

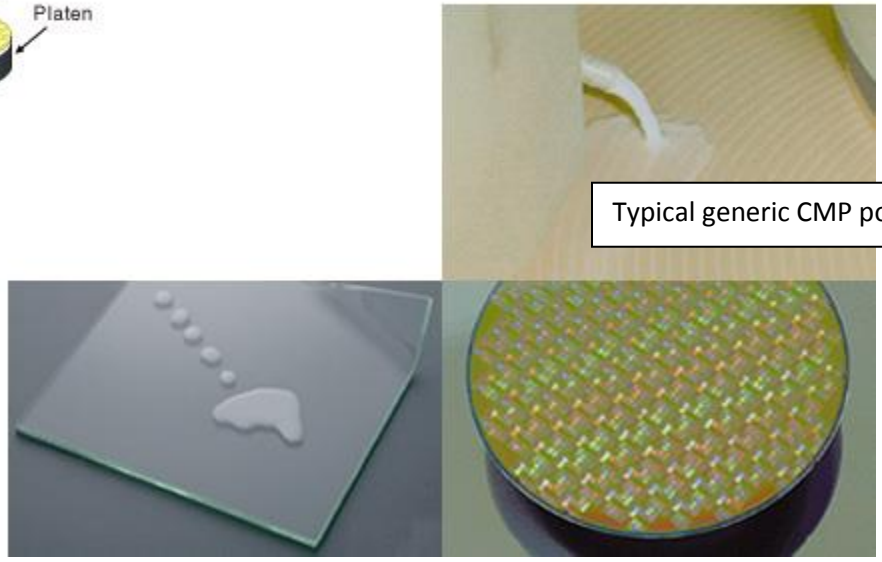
Multiple layers each individually planarized by the CMP process

Pictures used with permission from the MEMS Journal www.MEMSJournal.com

The Paradigm Shift Begins

Here is where one of the most radical and most important paradigm shifts in the history of semiconductor manufacturing came in. In the spring of 1983, a man named Dr. Klaus Beyer of the IBM Corporation, was trying to solve a stubborn problem related to post-polish cleaning of prime semiconductor substrates, wafers with no circuit patterns on them yet, but ready to be put into the manufacturing line to be made into computer chips. Because he also was trying to solve another problem at the same time, he also had a few device wafers, wafers ready to be diced into chips, wafers with humps and bumps from the deposition of the silicon dioxide insulator layer, often called "product wafers," so he decided to also polish those. He worked in a rather clandestine manner, late at night, on his own time, because he did not want to worry his manager. At that time, no one was allowed to touch the device side of the wafer with anything! Only a fool, or someone eager to be fired would dare to do what Dr. Klaus Beyer did next, but Klaus is no fool. Using a polishing machine that during the day time was used to polish the scratch-free surface of a silicon substrate (prime wafer), he put the pristine device side of the "product" wafer down onto a rotating polishing pad, and sprinkled some water-based colloidal abrasive slurry on it, and he polished.

Typical generic CMP polishing machine layout



Pictures courtesy of Asahi Glass Corp.

Upon examination, he found that the humps and bumps were gone! The topography that was causing major problems when trying to focus the image for follow-on layers of metal circuitry was eliminated. At that moment, Chemical Mechanical Polishing for the Planarization of Thin Films (CMP) was born. People had been polishing hard, brittle materials for thousands of years, but this was the first time anyone tried to polish the device side of the semiconductor wafer that was covered with materials of such dissimilar hardnesses such as aluminum or tungsten for the metal conducting layers, (copper now is common), polysilicon for the semiconducting layers, and glass for the insulator layers.

After a few days had passed, and under careful consideration about his future at IBM, he told his managers what he had done and what he had discovered in the process. Then he waited, expecting the worst. He expected that IBM would ask him to leave the company and pursue another career somewhere else; that being the anticipated and serious consequence of touching the device side of the wafer with anything let alone an abrasive coated polishing pad.

However, something amazing happened. Because of his discovery, IBM almost immediately put this process into their manufacturing line because it solved the challenge of planarization for their next generation of chips and allowed the new advanced microlithography systems just coming on line to focus properly and to successfully make the smaller and smaller features, i.e. the tiny copper wire lines and associated electronic devices. Klaus had solved the problem.

With modern machines built specifically for the CMP process, and advances in the CMP polishing pads, and the CMP polishing slurries, plus years of technical knowhow and scholarly investigation, the thin layers of insulating glass are now being polished to a final thickness of just a few hundred Angstroms or even less, and the layers of copper that build the wires and interconnection points, are planarized (leveled) to nearly imperceptible surface variations. One glaring lesson from Dr. Beyer's experiment is that he did not let conventional wisdom form a blockade and hinder his desire to advance the technology of the day. He did not stop at the norm.

CMP: The Enabling Technology

The discovery of CMP, led to the ability to begin building multiple layers of electronic circuitry on the silicon surface. This led to microlithography systems that had shorter and shorter focal budgets which meant that smaller and smaller lines and devices could be made in a full-scale manufacturing environment. Manufacturing circuitry with the CMP technology led to such rapid growth that manufacturing leap-frogged over research. Manufacturing lines were going in before companies set up the previously thought necessary research and

development operations to prove out this new process. The entire industry started to move at break-neck speed to bring Chemical Mechanical Polishing into their previously pristine manufacturing facilities. Abrasive slurries were brought into Class 100 clean rooms. Polyurethane polishing pads, normally considered "particle generators" and unwelcome in wafer fabs, were now out in the open fab environment. People walked around with CMP on their brains and colloidal silica under their fingernails. Gloves, cleanroom "bunny" suits, and covered facial hair became mandatory. In some parts of the fab, even self-contained oxygen systems are now required to minimize the negative effects of humans exhausting air into the environment. Complete rewrites of clean room protocol were required. Nearly overnight, people had to start thinking differently.

Rarely in today's world, is a state-of-the-art technology that was far advanced 30+ years ago, considered still to be state-of-the-art technology today. An exception is Chemical Mechanical Polishing, specifically for the planarization of thin films on semiconductor wafers, a process that has become mainstream and critical to chip manufacturing. CMP has spread to nearly all of the semiconductor manufacturing facilities around the globe. Now, virtually every semiconductor chip is manufactured using CMP techniques many times over, at least once for each conducting, each insulating, and each semiconducting layer that is placed on the wafer surface. Eighteen to twenty and even more ultra-thin layers of circuitry (copper conducting layers) are common now, and that means each layer (each metal conducting layer, each glass insulator layer, and each polysilicon semiconducting layer) must go through the CMP process. The basic consumables, while much refined and much improved over the years, are still quite similar to the consumables Dr. Beyer used those many years ago: a polishing pad, an abrasive slurry, then the application of pressure, and the speed of a rotating polishing platen, and there you have it: the recipe for the CMP process. Keeping in mind the fact that CMP was really not needed in semiconductor manufacturing until the devices, the metal lines, were being shrunk below 0.5 microns, a curious set of events is happening now in other parts of the digital device world.

Common Everyday Applications

There are approximately 6.5 billion cell phones in the world, nearly one for every man, woman, and child on the face of the earth. Every cell phone has chips in it that went through the CMP process.

There are 1 billion tablets being used every day and night by kids of all ages from 1-year olds to 100 years olds. There will be 5 billion tablet-based devices in less than ten years. Every tablet has chips in it that went through the CMP process.

There are over 1 billion automobiles on streets, roads, and highways all over the world and each one has multiple microprocessors on board, some as many as 100 or even more; and that number is going to increase

dramatically in coming years. Each of these microprocessors is made up of chips that went through the CMP process.

The huge opportunities that exist because of the "Internet of Things" (the I.O.T.) is staggering and is being made possible because of the ability now available to integrate several micro-scale devices and make them portable, and nearly self-sustaining. There are now 5 billion "things" actively connected to the internet, and this does not include the aforementioned cell phones and computers. This number is expected to grow to 20 billion "things" by the year 2020. So, if we have all of these "things" communicating can we measure how much communication is going on? How many bytes (units of digital information) are being transferred, i.e. exchanged around this world? Between mobile computing and the I.O.T., it has been estimated that two Zettabytes of data will be pushed through the internet this year, with that number growing to seven Zettabytes by 2017. In mathematical terms, that is $7x10^{21}$ bytes of data, or 70,000,000,000,000,000,000,000 bytes. (Source: "Silicon Photonics in a 300mm Fab – This is Getting Serious!" SemiWiki.com 13 May 2016, Mitch Heins).

Much of this information is gathered by sensors, and sensors are seemingly available everywhere for duplicating the five senses of the human body. Pressure sensors, temperature sensors, humidity sensors, acceleration and deceleration sensors, visual and infrared sensors, altitude sensors, directional sensors, and the list goes on and on, have been miniaturized to the point that they can now be unobtrusive to our everyday lives. We can wear them and not even know we are wearing them. They can be integrated into any number of devices to help us be safer, to help us learn better, to help us feel better, to monitor our physical condition in normal and emergency situations, to dispense the exact amount of medicine at exactly the right moment to ward off heart attacks, panic attacks, diabetic concerns, and other major health issues.

Not only are the small chips in these devices requiring the CMP process because their conducting lines are so small (well under the 0.5 micron threshold for CMP adoption), for every sensor there must be at least one semiconductor chip that is also manufactured using CMP techniques to provide memory and logic to take the information gathered by the tiny sensor and make some sense of it and put it to good use. The new technical devices that bring together micro-sensors with semiconductor logic and memory chips, "MEMS devices," can combine preventive and corrective medicine with semiconductor technology, emission control and abatement with semiconductor technology, accelerometers and gyroscopes with semiconductor technology, and the list goes on and on.

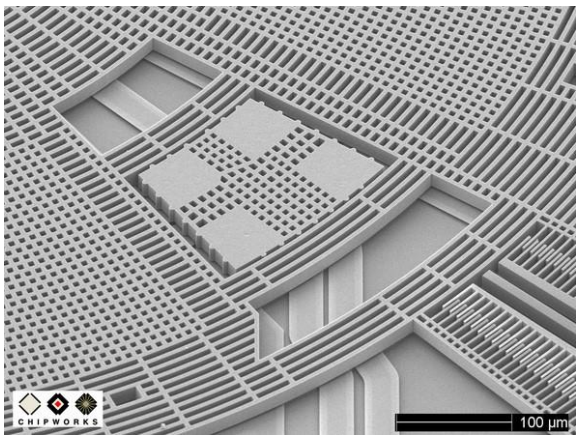
MEMS Devices – Real World CMP Applications

In military applications, the fundamental improvements made available because of processes like CMP, are easy to understand. This is due in large part to devices known as "MEMS" devices (Micro-Electro-Mechanical-Systems), and "MOEMS" (Micro-Optical-Electro-Mechanical-Systems). To better understand the concept of MEMS technology and MEMS devices, consider the common cell phone, the mobile communication device that none of us seem to be able to live without. Inside the typical, generic, commercially available cell phone, it is not unusual to find at least the following MEMS-based sensors and actuators:

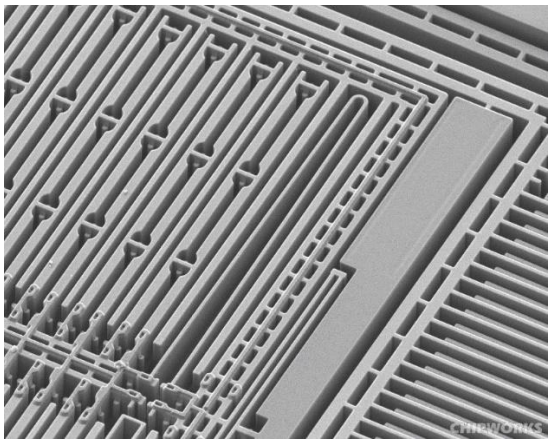
MEMS accelerometers	MEMS gyroscopes	Magnetometers
6-axis E-compass	6-axis Inertial Measurement Unit	9-axis combo solution system (Android)
Pressure sensors	MEMS microphones	Balk Acoustic Wave filters and duplexers
MEMS switches/variable capacitors	Silicon MEMS oscillators/resonators	Micro-mirrors
Microdisplays	MEMS autofocus mechanisms	Infra-red sensors
Humidity sensors	Temperature sensors	Image sensors
Fingerprint sensors	Still-camera technology	Video-camera technology
MEMS based micro-speakers	MEMS timing devices	Thermal imagers

Military hardware is more sophisticated than ever before and must be more reliable than our generic cell phones. In addition, weight is a major issue in systems such as aircraft, missiles and missile guidance systems, above water and below surface vehicles, tanks and armored personnel carriers, drones where weight and airborne longevity are extremely critical, and even more. Manufacturers of these vehicles and the spare parts needed to maintain them, are constantly making exciting steps forward to reduce the shear mass that these systems possess. One way is to reduce the size of the components and their component parts. This is where the CMP process, used to manufacture the advanced semiconductor chips that are used to make the sophisticated communication, GPS, and inertial guidance systems (MEMS) possible, comes into play. These digital devices, with their associated and interconnected semiconductor chips that now also have conducting lines much smaller than the threshold mark of 0.5 microns, and also have multiple layers of features and circuitry, need the CMP process.

MEMS-based iPhone® Gyroscope sensor; photo courtesy of Chipworks Inc. NOTE: A typical human hair is 100 µm (microns) in diameter.



MEMS-based Accelerometer sensor; photo courtesy of Chipworks Inc.



Combat Infantry Soldier

Take for example the type of equipment that the modern soldier carries. Reducing the weight and the size of the many items they carry with them helps reduce fatigue, helps improve mobility, and helps enhance

effectiveness. Items such as night vision goggles, head sets, radios, flash lights, beacons, solar power generators, GPS guidance and location systems, advanced heat generating and moisture dissipating fabrics, universally interchangeable batteries, fuel cells, and other digital devices along with their normal everyday necessities brings the load to 60 – 80 pounds or more.

Ironically, the amount of weight is not that far removed from the weight a World War I infantry solder was expected to carry. His load was made up of a steel helmet, gas mask, boots, canteen shaving kit, Springfield rifle, bayonet, knife, fork, spoon and one ration of food. That load would also have been about 60 pounds or so but what a contrast in technology between the load the World War I soldier carried versus that carried by the soldier of today. In mobile communications alone, great advances have been made in speaker technology, microphone technology, satellite based communication technology, GPS technology, accelerometer technology, gyroscope technology, battery technology, and on and on (just think once again about the many applications on your own cell phone), yet all of these advances are in a small, lightweight and very portable unit, many times smaller and lighter than previous field combat soldiers had to carry. Much of this is due to advances in digital technology, and much of that is due to advances in the CMP process.

Conclusion

Once again, the digital world is exploding! Personal computing has grown and matured and while the most amazing semiconductor manufacturing technologies are integral and internal to every computer, the technologies of this phenomenon now touch so many additional aspects of our daily lives, especially in the medical field, in personal hand-held communications devices, in the automotive industry, plus offering an important advantage in military and defense applications.

There does not seem to be any end in sight. CMP was introduced when feature sizes were larger than 0.5 microns, (500 nanometers, as huge as a house by today's standards). CMP continues to be enabling and critical to the manufacture of devices with feature sizes in the 22 nm range. CMP is being used in R&D labs today, where research is being done on feature sizes of 5 nm. CMP researchers, suppliers, and users, continue to make evolutionary improvements keeping the CMP process on the leading-edge of the technology. The semiconductor industry is famous and at the same time a bit notorious for extending the life of materials and processing techniques used in manufacturing the tiniest of conducting lines, the quickest of solid state devices, and the most reliable interconnects. These technologies need and use CMP every day in virtually every fab, everywhere. As the Internet-of-Things continues to grow (and some say it has not really even started its growth spurt yet), and as we continue to have this seemingly insatiable desire to be digitally communicative with any

one we please at any time we please, CMP is still going to be the enabling technology. Gadgets you can hold in your hand or wear on your sleeve, or imbed in your shoe are going to be more and more pervasive. Medical devices that measure your vital statistics and monitor your static and dynamic performance are in the process of multiplying to the point that every serious professional athlete and many neighborhood amateur athlete wanna-bees will have many of these devices integrated into their jerseys, socks, sunglasses, and pole vault poles to help improve performance. In hospitals and clinics worldwide, better, quicker, and more accurate diagnoses will be possible as these tiny MEMS sensors and devices assist the medical professional help you get back into good health and functionality. At the military and defense level, there is huge potential for growth in advanced equipment and devices that incorporate the latest semiconductor technology including the CMP process to manufacture instrumentation, aircraft, ships, land-based vehicles, personal wearables, weaponry, and more, all needed and necessary in the discovery, pursuit, containment, and if necessary, the attack and subduing of the enemy.

In a modern wafer fab, one may argue that none of the other 400 – 600 sequential manufacturing process steps appears to the uninitiated as being more Neanderthal-like than the Chemical Mechanical Polishing process. However, CMP now represents a multi-billion-dollar segment of the semiconductor manufacturing industry. Combining chemistry with the mechanics of the polishing process, rubbing a wafer on a polishing pad with some colloidal abrasive flowing about was extremely radical at one time but is commonplace and necessary today.

The fact is that nothing is more universally accepted as an enabling technology in semiconductor, MEMS, MOEMS, and nanotechnology, and nothing is more challenging in chip manufacturing, and nothing is more responsible for the absolute growth in the digital world than the CMP process.

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